VIAVI Solutions

Data Sheet

VIAVI

ONT-600 CFP2 Transport Test Module

Supporting 25G, 40G, 50G, and 100G Rates

The VIAVI™ ONT-600 CFP2 Transport Test Modules address all second-generation 4 x 25G/28G based 100G challenges. A wide range of transponders, such as CFP2, CFP4, QSFP28 and SFP28, is supported. Its unique applications probe deep into the physical layer. The available electrical adapters enable troubleshooting and service verification tests on board level in labs. The CFP2 Transport Test Module is a key enabler bringing transport components and systems to market faster and more reliably.

The CFP2 Module, based on 25/28G input/output (I/O) technology, is critical for driving mass deployment of 100G cost-effectively. While the first-generation 100G CFP was based on 10G I/O, CFP2 density and price drivers require deploying novel 25/28G technology, challenging everyone from integrated circuits (IC) and optical module vendors through equipment manufacturers. Signal integrity and physical layer considerations add more complexity.

Key Features

- Supports wide range of transport bit rates, from 25 Gbps to 112 Gbps
- Native support for CFP2 and QSFP+
- SFP28, CFP4, QSFP28 form factors and electrical access supported by adapters
- Physical test features, dynamic skew variation, jitter insertion, advanced error analysis, MDIO/ I²C access
- Comprehensive troubleshooting tools at PCS/ Ethernet and multiplexed OTN signals and their clients
- Fully independent dual-port test with OTN/ Ethernet drop-and-insert functionality

Key Benefits

- Securing investments by future-proof platform
- All-in one solution provides flexibility to utilize platform for a variety of transponders and technologies
- Pre-qualification and in-depth validation of transponders and receivers for type approval and production
- Simplification and acceleration of System Verification Testing (SVT) while maintaining test depth
- Mapping/de-mapping bulk, Ethernet or SDH/SONET clients into complex OTN MUX structures

Applications

- System development: The VIAVI CFP2 Transport Test Module covers the physical layer through to PCS, Ethernet/IP, SDH/SONET and OTN, making it the ideal tool for hardware and software developers to proof their designs. In system verification labs, it leaves no area uncovered, and with its leading-edge automation support it is helping Network Equipment Manufacturers to bring new 100G systems to market quickly and with greater confidence.
- Transponder test: Support for CFP2/CFP4/QSFP28/SFP28 modules with MDIO/I²C debugging and single-button CFP2 Stress test applications help develop and validate modules to challenging standard requirements, like dynamic skew tolerance.
- IC development and validation test: A powerful, flexible electrical interface (via active CFP2 electrical adapter) with wide ranging physical-layer applications and comprehensive troubleshooting tools for signal integrity, PCS, Ethernet, and OTN traffic using real-world traffic rather than limited, unframed PRBS signals to validate performance.
- Manufacturing test: A less expensive version is available that is optimized specifically for manufacturing and SVT applications (ONT-602). The comprehensive and fast automation provides higher production output without compromising test depth.

Additional Features

- Industry's most complete Transport Test Module
- Native support for 4x25/28G I/O used in CFP2, CFP4, QSFP28 and 100G ASICS and FPGAs
- High-performance active electrical adapter and powerful applications to support other technologies based on 25/28G I/O
- Includes all the key features component manufacturers require with many unique applications for validating ICs and transponders at 25/28G
- Unique physical-layer applications that quickly identify the root cause of errors with complete coverage from signal integrity through to CDR issues, timing, and pattern sensitivity
- 25GE, 40GE and 100GE Ethernet generation and analysis capabilities including:
  - various frame formats and sizes
  - RFC 2544 test suite
  - IPv4 and IPv6 support with up to 256 streams
  - MPLS, VLAN, and QinQ support
  - native Ethernet as well as full Ethernet client functionality in OTN
- Comprehensively tests and validates QSFP28 modules, components, and SR4, PSM4, CWDM4, SWDM4, LR4 interfaces as well as validates line card RS FEC implementation and performance
- Simultaneously conduct 40GE/OTU3 or 100GE/OTU4 dual-port tests for SVT or manufacturing applications
- Industry's most complete OTN multiplexing test depth
- Unique solution for testing PTP 1588v2 at 40GE and 100GE
- SR4 FEC validation option verifies and stresses RS FEC core implementations

Additional Benefits

- All-in one solution cuts costs for new system development and production with configurable tests for the physical layer through to PCS, Ethernet, OTN and PTP 1588v2 applications
- Verification of master-slave delay and PDV accuracy for Carrier Ethernet and Mobile Backhaul applications
- All-in one solution provides flexibility to utilize platform for different transponders and technologies
- One-box solution combines flexible generation and real-time analytics in one simple-to-use and economic solution
- In-depth testing of Ethernet and real-life payloads within ODU channels
- Provides best-in-class tools for rapid and comprehensive debugging of protocol and 25/28G physical layer issues

Mainframe Hardware Configurations

The VIAVI CFP2 Transport Test Module benefits from experience with our industry- reference ONT CFP module, a powerful 40/100G core engine that blends high-performance I/O with our far-reaching, leading applications from the physical layer through complex OTN applications. This ensures that high-fidelity 25/28G signals and their clock sources will underpin all second-generation 100G technology. Low jitter and low phase noise I/O on the front panel provide confidence in signal integrity. The test solution can scale as customer needs increase, first focusing on validation of the physical layer and then comprehensive applications for Ethernet/IP and OTN.

Various ONT CFP2 solution configurations are available that address the needs of IC vendors, optical module vendors, network equipment manufacturers, or service provider labs. The various configurations offer applications used in design verification; hardware, software, and SVT; and manufacturing. It can be purchased as a modular solution for ONT-603, -606, or -612 mainframes or as a rack-mounted point solution called the ONT-602.

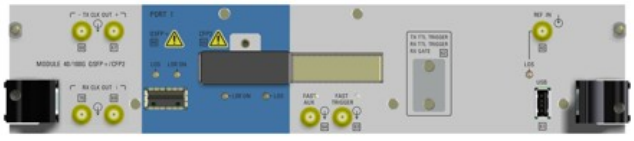
Dual-port CFP2 plugged into ONT-603 Mainframe

19" ONT-612 Rack Mount mainframe - houses up to 6 CFP2 modules or combination of other ONT modules

CFP2 Transport Test Modules

CFP2 Phy/Data Single Port Module (BN 3076/92.80)

The CFP2 Phy/Data Single Port Module offers the complete in-depth test capabilities needed for physical layer R&D applications, including dynamic skew insertion, jitter injection, advanced error analysis and many more. In addition, it covers the complete range of CFP2 based OTN, Ethernet and SDH/SONET testing in R&D, SVT and Manufacturing.



Front Panel of CFP2 Single Port Phy/Data Module

CFP2 Phy/Data Dual Port Module (BN 3076/92.83)

The CFP2 Phy/Data Dual Port Module offers the complete, in-depth test capabilities needed for physical layer R&D applications, including dynamic skew insertion, jitter injection, advanced error analysis and many more. In addition, its second port allows for bidirectional OTN monitoring with Through Mode and can add/drop Ethernet client signals to/from OTN high-speed signals for further evaluation. Covers the complete range of CFP2 based OTN, Ethernet and SDH/SONET testing in R&D, SVT and Manufacturing.

Front Panel of CFP2 Dual Port Phy/Data Module

ID	Function	In/Out	Type	Comment
[60]	REF IN	IN	50 Ω SMA	f/40 or f/160 selectable
[61]	USB 2.0	IN/OUT	A-coded USB socket	Internal use
[62]	TTL Trigger I/O			
[63]	FAST TRIGGER	OUT	50 Ω SMA	
[64]	FAST AUX	OUT	optical	f/4
[65]	CFP2 cage, port 1	IN/OUT	optical	CFP2 MSA compatible pluggables
[66]	QSFP+ cage, port 1	IN/OUT	optical	QSFP+ MSA compatible pluggables
[67/68]	TX CLK OUT	OUT	50 Ω SMA	f/40 or f/160 selectable
[69/70]	RX CLK OUT	OUT	50 Ω SMA	
[71]	QSFP+ cage, port 2	IN/OUT	optical	QSFP+ MSA compatible pluggables
[72]	CFP2 cage, port 2	IN/OUT	optical	CFP2 MSA compatible pluggables

f = CAUI/XLAUI Electrical lane speed

[71] and [72] only for CFP2 Dual Port Module

Hardware Adapters and Transponders

The CFP2 Module has one or two native CFP2 cages (4 x 28G based) and QSFP+ cages (4 x 10G based). A variety of transponders and adapters is available for the 4 x 28G based cage(s).

Using the available phy-level electrical adapter, in-depth physical layer testing of transponders and evaluation boards is possible via port 1 of the CFP2 Phy modules.

The "Basic electrical adapter" can be used in port 1, but also in port 1 and 2 in parallel, mainly for manufacturing applications.

Other adapters are available to accommodate different form factor transponders such as QSFP28, SFP28 or CFP4.

CFP2 to CFP4 Passive Adapter (BN 3076/92.92)

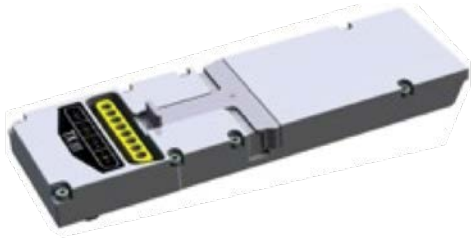
This adapter lets you operate a CFP4 transponder inside the CFP2 cage. Full management access via the ONT GUI. Can operate in ports 1 and 2.

CFP2 to QSFP28 Active Adapter 3076/92.93

This adapter lets you operate a QSFP (4x28G) transponder inside the CFP2 cage. It also gives full management access from the ONT GUI via the I2C interface (instead of the MDIO which is used with CFP2 transponders). Can operate in ports 1 and 2.

CFP2 to SFP28 Active Adapter (BN 3076/92.98)

Allows to operate an SFP28 Transponder inside the CFP2 cage. Supports one 25GE per port. Can operate in ports 1 and 2



CFP2 Basic 4x25G Electrical Adapter (BN 3076/92.94)

Basic electrical access to 4x25G interface, will work in Port 1 and 2 of ONT CFP2 Phy and Data modules. Cable set not included in Basic Electrical Adapter.

Active CFP2 electrical adapter to test external devices such as ICs and modules based on 25/28G I/O.

Electrical interface consists of two Huber+Suhner MXP series 8 x 1 connectors. 8 coax cable assembly to be provided by customer.

Connector 1	RX CAUI4 (4 lanes differential)
Connector 2	TX CAUI4 (4 lanes differential)

CFP2 4x25G Electrical Adapter (BN 3076/92.90)

- With Wideband Jitter insertion and recovered clock output
- Electrical access to 4x25 interface, includes 4 times K1002 (8 coax cable assembly), will work in Port 1 only of ONT CFP2 Phy modules
- High-performance active CFP2 electrical adapter, works with the ONT CFP2 module to test external devices such as ICs and modules based on 25/28G I/O. GUI access to MDIO interface of external eval-board is possible via optional cable K1001. With Wideband Jitter insertion and recovered clock output
- Dynamic skew insertion and low-band jitter injection work as before.
- Supports wideband jitter inject on one TX lane with an external modulation signal connected to the modulation input of the CFP2 electrical adapter

Jitter modulation range: 30 kHz - 1 GHz, with 2 UIpp maximum amplitude

Electrical connectors: three Huber+Suhner MXP series 8 x 1 cable assemblies.

Connector 1	RX CAUI4 (4 lanes, differential)
Connector 2	TX CAUI4 (4 lanes, differential)
Connector 3	Auxiliary connector with jitter injection input, reference CDR Out, and TX CAUI4 (lane 3) with added jitter

Physical Layer Testing

Physical Layer

CFP2 Interface (4 x 25/28G based)	
103.125 Gbps (100G Ethernet) and 111.81 Gbps (OTU4)	
In accordance with CFP2 MSA 2.0	
Reference clock	CAUI4 (CFP2) 1/40, 1/160, MAC rate (156.25 MHz)
Power class	1,2,3,4
MDIO modes	Internal normal, internal relaxed, and external
MDIO functionality	A-page, 2.0, and some 2.2 enhancements
MDIO speed	Slow (500 kHz), normal (2 MHz), and fast (4 MHz)
I^2C Speed (with QSFP28 adapter and SFP28 adapter):	Slow (100 kHz), normal (200 kHz), and fast (400 kHz)

QSFP+ Interface (4 x 10G based)
Supported bit rates: 39.81 Gbps (SDH/SONET, unframed), 41.25 Gbps (40G Ethernet), 43.018 Gbps (OTU3), 44.57 Gbps (OTU3e1 bulk and unframed), and 44.58 Gbps (OTU3e2 bulk and unframed)
Adjustable in 0.01 ppm increments up to a range of ±500 ppm (depends on transponder used)
In accordance with QSFP+ MSA3.5
Support for power classes 1, 2, 3, 4 (3.5 W maximum power)
Electrical data interface XLIPPI according to IEEE 802.3ba
Clock Source
Internal reference, recovered from Rx, external clock source via mainframe clock input or via high-speed sync clock input (differential or single-ended), adjustable clock bandwidth supported on sync clock input (<100 Hz, ~1 MHz, >15 MHz). The clock bandwidth can be controlled through the relevant application GUI.
Tx Clock Output
SMA output, nominal level is 1200 mV into 100 ohm, differential. Single-ended can be used when terminating unused output with 50 ohm. Note: Clock recovery lane is always lane 0.

Tx Reference Clock	
XLAUI (QSFP+)	Electrical lane speed /16 or /64
CAUI4 (CFP2)	Electrical lane speed /40 or /160
Rx Recovered Clock	
XLAUI (QSFP+)	Electrical lane speed /16 or /64
CAUI4 (CFP2)	Electrical lane speed /40 or /160
CFP2 Tx MCLK	
According to MSA	

Rx Clock Output
SMA output, nominal level is 1200 mV into 100 ohm, differential. Single-ended can be used when terminating unused output with 50 ohm.

Modes	
CFP2 Rx MCLK	According to MSA
Rx Eye Clock	From lanes 0, 1, 2, 3
"Golden PLL"	Electrical lane speed divided by 8, 16, 32, 64, or 128
Bandwidth selection	Low < 5 MHz Normal ~10 MHz High > 15 MHz
Fast trigger output	
Pattern trigger	SMA, 600 mV into 50 ohm

Physical Layer Functionality		
Unframed 4-channel BERT		
Data Rates Supported		
Applications	***Bit Rate (Gbps)***	***Lane Speed (Gbps)***
40 G (QSFP+)		
OC-768	39.8131	9.95328
Ethernet	41.25	10.3125
OTU3	43.01841	10.7546
OTU3e1	44.57097	11.1427
OTU3e2	44.5833	11.14583
100 G (CFP2)		
Ethernet	103.125	25.78125
OTU4	111.089	27.77

BERT Testing	
Tx patterns	PRBS7, -9, -15, -23, -31 and inverted, 32 Bit DW, SSPR, square wave
Pattern lane offset	None, auto staggered, user-defined
Bit error insertion	On selected lane, all lanes
Rx patterns	PRBS7, -9, -15, -23, -31 and inverted, SSPR, 32 Bit DW
Bit error analysis	Total, errored 1 or 0, ratio
Gating modes	Manual start/stop, predefined duration, intermediate time
Lane Operation Modes	
QSFP+	Per lane, each 4 x 10G lane is a separate channel
CFP2	Per lane, each 25/28G lane is a separate channel with same type of pattern Independent lane, each 25/28G lane can independently choose PRBS or digital word
4 x (5 x 5 G) mode	Each lane contains five independent bit-multiplexed signals with pattern transparency for CFP and CFP2 gearbox-based implementations. This mode can interoperate with the ONT CFP 10x(2x5G) mode for true end-to-end gearbox testing.

User-entered bit rate 25 – 28 Gbps (BN 3076/94.34)

Lets users set arbitrary 25.3 to 28.05 Gbps per lane with 1 kbps (~0.01 ppm) resolution.

Hardware Validation (BN 3076/94.30)

The Hardware Validation option adds these capabilities:

- CFP2 debug, including MDIO and CFP2 validation
- Clock-frequency-variation application
- CAUI4 control over TX pre-emphasis and RX gain and slicer level
- Lambda-mapping application

Hardware validation is required for applications such as dynamic-skew variation and advanced error analysis.

External MDIO and Auxiliary Triggers

Access to the external transponder evaluation board's MDIO interface

Auxiliary bit error trigger and gating control, 3.3 V positive logic

Optional adapter cable (K1001) required

CAUI4 Control

General

CFP2 interface supports 4 lanes, differential RX and TX with control of TX and RX functionality.
TX can be muted and both TX and RX lanes can be inverted. CAUI4 interface is AC coupled with LF cutoff of ~ 30 kHz.

TX Pre-Emphasis Settings

Modes	Normal, high, and user-defined
Normal precursor	400 mV and main = 400 mV
High precursor	570 mV and main = 400 mV
User-defined (with coupled or separate lanes)	Setting range is 200 mV to 1200 mV with 10 mV resolution

RX Equalization

Modes	Normal and user-defined

User-defined lets users set equalization from 0 to 7 dB with 1 dB resolution, lanes can be separate or coupled.

Data Slicer Level

Modes	Normal and user-defined

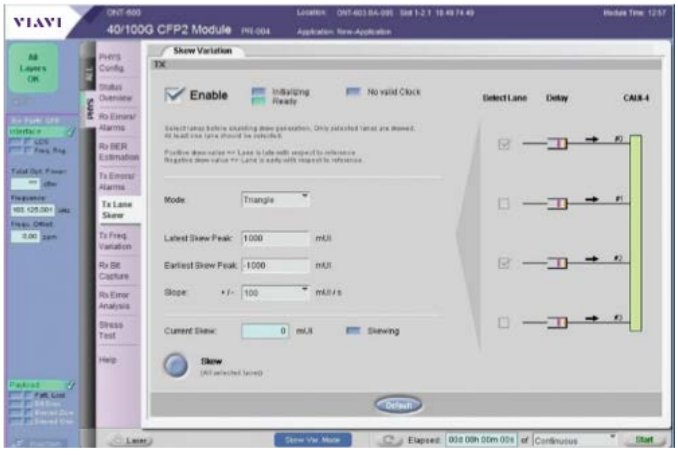
User-defined setting can be adjusted from –200 to + 200 mV, with 0 mV as the default.

Dynamic Skew Variation (BN 3076/94.32)

Requires option BN 3076/94.30 (hardware validation).
The CFP2 Dynamic Skew Variation option lets users vary the relative skew in individual data lanes over a ±512 bit range in increments as small as 10 mUI.

Modes	Manual or triangle
Clock source	Internal or external
Skew slope	Selectable from 10, 20, 50, 100, 200, 500, 1000, 10000 mUI/s
Range	±512 U

Calibration and de-skew is carried out when the dynamic skew mode is first enabled or if the bit rate is changed. During this process, the TX output signal may be disrupted.



Dynamic skew overview screen

Advanced Error Analysis (BN 3076/94.31)

Requires option BN 3076/94.30 (hardware validation). The advanced error analysis option is a unique set of applications designed to accelerate troubleshooting, fault-finding, and stress testing of 25G+ hardware. It gives unique insight into the very nature of errors and, with clear indications of the patterns and statistics of the errors, it enables root causes to be quickly identified.

Applications include investigating CDR and FIFO slips, hardware pattern sensitivity, and error burst profiling

Bit Capture

The bit capture application allows each lane to be captured to a depth of 512 kbits per lane. The capture occurs after the trigger event.

Bit capture screen

Trigger: manual (via force trigger on GUI), error (any lane or user selected lane), external trigger event (front panel SMA connector [62]). Trigger can be single shot or continuous. Bit errors can also be set to cause a trigger event at the fast trigger output on the front panel. This can be used to trigger external devices (real-time fast oscilloscopes) to allow the physical and logical domains to be compared together to help error cause investigation. Bit errors are indicated by red shading on the errored bit on the GUI. User controls allow scrolling and zoom in/out of view portion of captured pattern.

A captured bit pattern can be saved as a CSV file.

RX Error Analysis

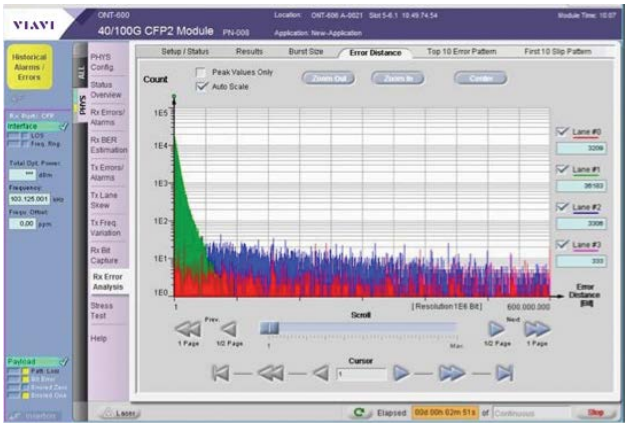
The advanced error analysis application reports the error distance distribution, and burst length distribution as graphs which can be viewed, zoomed, and scaled by the user. Error patterns that caused the highest number of bit errors are captured and displayed to facilitate pattern-sensitivity investigations. The top 10 patterns leading up to bit-slip conditions are also captured and displayed to enable troubleshooting of issues around CDR and FIFO slips.

Advanced error analysis setup screen

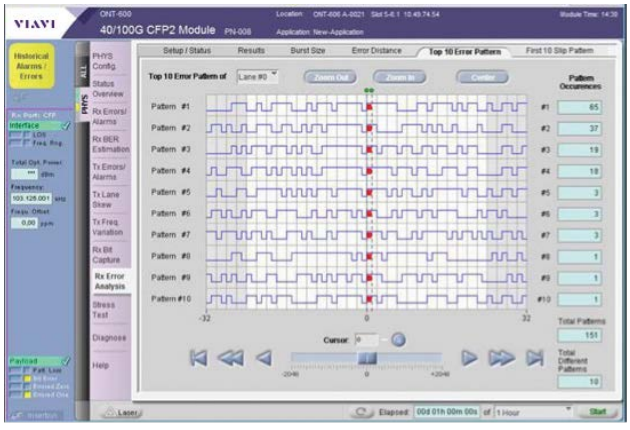
Advanced error analysis setup screen

Advanced error analysis screenshot showing each lane data analyzed for bit errors, burst errors, and bit slips

Each of the four lanes is color coded and can be turned on and off in the graphic as required. The user can scroll and zoom into the error distance profile to investigate the error type. Typical (random) errors should exhibit a Poisson-like profile while pattern-dependent or external crosstalk noise may cause discrete spectra.



Comparison of the error distance profile on each lane



Display of top 10 error patterns showing strong correlation with pattern type

Jitter Insertion (BN 3076/94.33)	
Allows user inject jitter on lane 3 of the optional electrical adapter (BN 3076/92.90)	
Jitter Modulation Input	
Connector	2.92 mm, 50 ohm, AC coupled
Modulation range	≤ ±40 ps
Sensitivity	≥160 ps/V
Frequency range	30 kHz to 1 GHz
MLG 1.0 Support (BN 3076/94.36)	
The Multi-Link Gearbox Analysis option for the ONT 100G CFP2 modules generates, monitors, and analyzes the performance of 10 individual 10GBase-R signals encoded over 25G I/O conforming to OIF MLG 1.0. This option also enables ONT 100G CFP2 modules to test MLG-enabled line cards on the 25G side (optical or electrical) while the ONT MTM module can be used to generate/analyze the individual 10GE	
Applications	Developing MLG ASIC, testing, and validating MLG pluggable optical modules as well as turning up and validating MLG-enabled line systems
Interfaces	The CFP2 interface natively supports MLG-enabled CFP2 modules, and it can support the MLG module and host ASICs through the CFP2 electrical interface. (BN 3076/92.90)
10GBase-R Encoding/Decoding	
10 user-selectable 10GBase-R links	
Disabled link transmit signal	Local fault, scrambled idle
MLG alarm generation/ detection	Loss of block lock, loss of alignment marker lock
MLG lane error insertion/ detection	Invalid sync header, invalid alignment marker, user-defined alignment marker, BIP-8 error, user lane ID
Static/dynamic skew range	The same as non-MLG mode (100GE)
PCS-Layer (per individual 10GE link)	
Minimum interpacket gap	8 to 127 bytes
Minimum interpacket gap threshold	5 to 255
Reconciliation alarm insertion	Local fault, remote fault
64/66B alarm insertion	LOBL, HiBER
64/66 error insertion	Invalid sync header, user control block, error propagation/E/

Statistics	
Reconciliation alarms (seconds)	Link down, local fault, remote fault, IPG violation
Reconciliation errors (count and rate)	Error propagation /E/, local fault events, remote fault events, IPG violation events
64B/66B alarms (seconds)	LOBL, HiBER
64/66 errors (count and rate)	Invalid sync header, errored block, invalid block, LOBL events, HiBER events
MAC/IP Layer in the MLG Application	
Supports one MAC flow per 10GE link.	
Ethernet Generator	
Frame type	Ethernet II, SNAP, VPLS with inner and outer MAC, MAC-in-MAC 802.1ah
Ethertype	Editable value
VLAN tagging	Single IEEE 802.1q, double (Q-in-Q) IEEE 802.1ad
Editable parameters	TPI, priority, CFI/DEI, VID
MAC addresses - Source and Destination	
MAC frame size	
Predefined frames	64, 128, 256, 512, 1 024, 1 280, 1 518, 2 000, 9 000, 9 600, 10 000 bytes
User-defined frames	64 bytes to 10 kbytes
Dynamic frame size	
VPLS framing	
MAC-in-MAC 802.1ah framing	
Payload type	VIAVI test frame, PRBS31, PRBS31 inverted
Traffic Generator	
Traffic control	
Mode	Bandwidth-controlled, gap-controlled
Trigger	Continuous, once (bandwidth- controlled)
Traffic type	Constant, burst, back-to-back, ramp, IMIX
Frame size	Editable, fixed values, dynamic increment/ decrement, random
MAC Error Insertion (per 10GE link)	
Error type	MAC, runt, oversized, FCS errored, invalid SFD)
Error type (test frame)	Loss, mis-insertion, duplication, swapping
Error type (test pattern)	Bit error

Generator Statistics	
Bandwidth	current and average, Mbps, %, plus graphics
Total byte count	
Total frame count and rate	
Pause frame count, rate, and ratio	
MAC bandwidth per flow current and average in bps	
Utilization per flow current and average in %	
Bytes per flow count	
Frames per flow count, rate, and ratio	
Ethernet Analyzer	
MAC Flow Filtering (per 10GE Link)	
Frame type	Ethernet II, SNAP, VPLS with inner and outer MAC, MAC-in-MAC 802.1ah
Ethertype	Editable value
VLAN tagging	
Type	Available for all frame types, single IEEE 802.1q, double (Q-in-Q) IEEE 802.1ad
Editable parameters	TPI, priority, CFI/DEI, VID
MAC addresses	
Destination address	Editable
Source address	Editable
VPLS framing	Supported, see Ethernet Generator
MAC-in-MAC framing	Supported, see Ethernet Generator
Total Link Analysis (non-flow selective)	
Error counts	
MAC frame/byte counts	
Pause quanta and time	
Bandwidth/utilization	
Frame size results	
Frame size distribution	
QoS Measurements (per 10GE link)	
QoS alarms and errors, throughput MAC/IP, transfer delay	
BERT measurements (per 10GE link)	
BERT alarms and errors	
Service Disruption Measurements (per 10GE link)	
Disruption results are given for any disruption that occurs above the disruption time threshold (10GE link selective).	
Packet Jitter Analysis (per 10GE link)	
Instantaneous jitter, jitter hits	

PCS and Ethernet Layers

PCS Layer	
40GE and 100GE only, supported by CFP2 or QSFP+ as appropriate.	
Each lane is clocked from common clock.	
TX/RX scrambler	On/off independent (only available for L2/L3 layer testing)
TX ignore link faults	On/off (only available for L2/L3 layer testing)
Payload	As follows or client signal from higher-layer application.
Pattern Modes	Virtual lane, aggregate
Virtual Lane Mode	
Pattern	PRBS7, -9, -15, - 23,-31 and inverted
TX lane offset	Auto staggered, user-defined offset
User-defined offset	10 to 64,000 bits (depends on PRBS pattern)
Aggregate Mode	
Pattern	Scrambled idles
Error Insertion	
Supports simultaneous error and alarm insertion	
Type	Invalid sync header, invalid alignment marker, user-defined alignment marker, BIP-8 error, bit error (all lanes/single lane), block error
Range (depends on type)	All lanes, single lane
Trigger	Once, rate, burst once/cont.
Rate	9.9×10^{-3} to 1×10^{-10}
Burst	N events off, M events on
N, M	1 up to 16,777,215 events
Sync header value	Editable 0 to 3
Alignment marker M0, M1, M2	Editable 0 to 255
BIP-8 error mask	Editable 0 to 255
Alarm Insertion	
Supports simultaneous error and alarm insertion	
Type	LOBL (loss of block lock), LOAML (loss of alignment marker), HI BER (high bit error rate), local and remote fault, bit error (total, per lane)
Range (depends on type)	All lanes, single lane
Trigger (depends on type)	Continuous, burst once/cont.
Burst	N events off, M events
N, M	8 up to 134,217,720 events (local and remote fault)

Error Evaluation	
Type	Invalid sync header, invalid alignment marker loss of alignment marker event, BIP-8 error, BIP-8 bit error, LOBL event, HI BER event, local and remote fault event, bit error (total, per lane), errored zero (total, per lane), errored one (total, per lane), block error
Evaluation (depends on type)	Count, ratio, rate, seconds summary and per lane
Alarm Evaluation	
Type	LOBL, summary, per lane, LOAML, LOA (loss of alignment), HI BER, local and remote fault, link down (only available for higher-layer testing) pattern loss
Evaluation	Seconds
Lane Alignment Marker Insertion PCS Lane Mapping	
For all virtual lanes	User-defined
TX lane mapping	User-programmable (shift)

MAC/IP Layer

Basic Ethernet Features	
Supports one MAC flow for TX and RX. Multistream is optional.	
Ethernet Generator	
Frame type	Ethernet II, SNAP, VPLS with inner and outer MAC, MAC-in-MAC 802.1ah
Ethertype	Editable value
VLAN Tagging	
Type	Available for all frame types single IEEE 802.1q, double (Q-in-Q) IEEE 802.1ad
Editable parameters	TPI, priority, CFI/DEI, VID
MAC Addresses	
Destination address	User-defined, multicast, broadcast
Source address	User-defined, factory default
MAC frame size	User-defined, jumbo
Predefined values	64, 128, 256, 512, 1,024, 1,280, 1,518, 2,000, 9,000, 9,600, 10,000 bytes
User defined	64 bytes to 10 kbytes
Dynamic frame size	Increment/decrement, random, maximum/minimum, user-defined
Selectable increment step size	1 to 10 kbytes

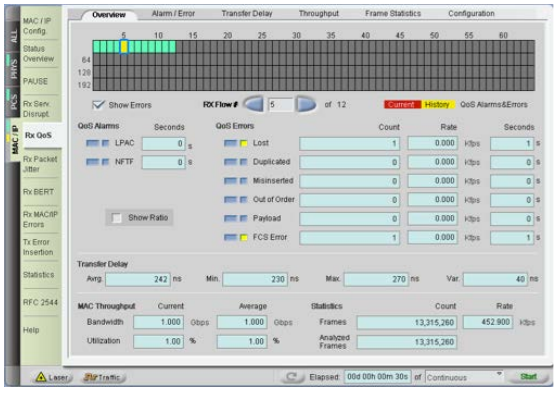
VPLS Framing	
Inner Frame Structure	
As per standard Ethernet frame, including MAC addresses, VLAN tags (2), frame type, Ethertype, and payload	
Outer Frame Structure	
Parameters	MAC addresses, frame type, Ethertype
Tunnel and VC label	Label, CoS, TTL
Control word	Reserved bits, sequence number
MAC-in-MAC 802.1ah Framing	
Inner Frame Structure	
As per standard Ethernet frame including MAC addresses, VLAN tags (2), frame type, Ethertype, and payload	
Outer Frame Structure (PBB/PBT)	
Parameters	MAC addresses
B-Tag	TPI, VID, priority, DEI
I-Tag	TPI, SID, priority, DEI, NCA, Res1, Res2
Payload of MAC Frames	
Type	VIAVI test frame, PRBS pattern
VIAVI test frame	Time stamp and sequence number
Filling pattern	Editable digital word, PRBS31
PRBS pattern	PRBS31 and inverted
	Up to 124 bytes of user payload are freely editable.
Flow Control	
Modes	Generation, emulation, analysis
Generation of PAUSE frames	Off, once, continuous
Once	Number of frames per shot 1 to 2^{16}
Pause frame interval	Editable 60 ns to 10 s
Pause quanta	Editable 0 to 64,000 (0 to 0.335 ms)
Emulation of flow control	Throttling on/off
Analysis of PAUSE frames	See analyzer
Traffic Generator	
Traffic Control	
Mode	Bandwidth-controlled, gap-controlled
Trigger	Continuous, once (bandwidth- controlled)
Continuous	Ongoing traffic as defined
Once	Triggers generation of programmed number of frames/bursts per flow (see traffic profiles—burst)
All flows are started synchronously	

Gap-Controlled Traffic	
Gives users precise and direct control over the IPG sequence generated. Resolution of 1 byte.	
Traffic Profile for Bandwidth-Controlled Traffic	
Each flow must be associated with one of 8 independent traffic profiles. Supports online updates of traffic profiles.	
Traffic type	Constant, burst, back-to-back, ramp, IMIX
Frame size	Editable, fixed values, dynamic increment/ decrement, random
Back-to-back (enables maximum bandwidth by forcing the traffic to minimum inter-packet gap)	On/off
Constant Mode	
Burst Mode	
Peak, sustained bandwidth	Adjustable utilization in Mbps and %
Burst size	1 to 64,000 frames
Utilization accuracy	0.1%
Traffic Profile for Gap-Controlled Traffic	
Traffic type	Constant IPG, increment/decrement IPG, random IPG
Frame size	Editable, fixed values, dynamic increment/ decrement and random
IPG constant	8 to 232 bytes
IPG increment/ decrement start/stop	Min to 2,047 bytes
IPG step size	1 to 64 bytes
IPG random minimum/ maximum values	Min to 2,047 bytes
MAC Error Insertion (any flow or per flow)	
Error type	MAC, runt, oversized, FCS errored, invalid SFD
Triggering	Once, continuous, burst once/burst cont.
Rate	9.9×10^{-3} to 1×10^{-9}
Burst	M errored, N non-errored frames
M, N	1 to 2^{24} frames
MAC Error Insertion (per flow only)	
Error type (test frame)	Loss, misinsertion, duplication, swapping
Error type (test pattern)	Bit error
Triggering	Once

Generator Statistics	
Bandwidth	Current and average, Mbps, %, plus graphics
Bytes total	Count
Frames total	Count and rate
Pause frames	Count, rate, ratio
MAC bandwidth per flow	Current and average in bps
Utilization per flow	Current and average in %
Bytes per flow	Count
Frames per flow	Count, rate, ratio
Ethernet Analyzer	
MAC Flow Filtering	
The flow filter defines the parameters that particular flows must fulfill to pass the filter and for detailed analyzed. Others are not looped through to the per-flow analysis. Offers undefined as well as defined values.	
Frame type	Ethernet II, SNAP, VPLS with inner and outer MAC, MAC-in-MAC 802.1ah
Ethertype	Editable value
VLAN Tagging	
Type	Available for all frame types, single IEEE 802.1q, double (Q-in-Q) IEEE 802.1ad
Editable parameters	TPI, priority, CFI/DEI, VID
MACAddresses	
Bandwidth	Adjustable utilization in Mbps and %
Utilization accuracy	0.1%
Destination address	Editable
Source address	Editable
VPLS framing	Supported, see Ethernet Generator
MAC-in-MAC framing	Supported, see Ethernet Generator
Total Link Analysis (non-flow selective)	
Error Counts	
MAC types	Errored, FCS errored, runt, oversized, invalid preamble, invalid SFD
Evaluation	Count, rate, ratio, seconds
MAC Frame/Byte Counts	
Bytes	Total
Frames	Total, good, errored, broadcast, multicast, pause
Evaluation (type dependent)	Count, rate, %, and graphics
Pause quanta and time	Last, min, max , count, rate, ratio

Bandwidth/Utilization	
Total used bandwidth and utilization	
Bandwidth	Current, average in Mbps
Utilization (used bandwidth/ link bandwidth)	Current, average in %
Frame Size	
Results	Min., max., average
Frame size distribution	Count, rate, ratio graphical display of results
Distribution classes	64, 65 to 127, 128 to 255, 256 to 511, 512 to 1,023, 1,024 to 2,000, >2,000 bytes
Analysis per flow	
Filtered-in Bandwidth	
Evaluation of the Traffic Flows	
Bandwidth of all filtered flows	
Bandwidth	Current, average in Mbps
Utilization (used bandwidth/ link bandwidth)	Current, average in %
Bandwidth/Utilization Measurements per Flow	
Bandwidth of single filtered flows	
Types	Current MAC, current payload, average MAC, average payload
Bandwidth (used bandwidth/ link bandwidth)	Mbps
Utilization (link)	in %
Frame Counts per Flow	
Types	Bytes, frames
Evaluation	Count, rate, ratio
QoS Measurements per Flow	

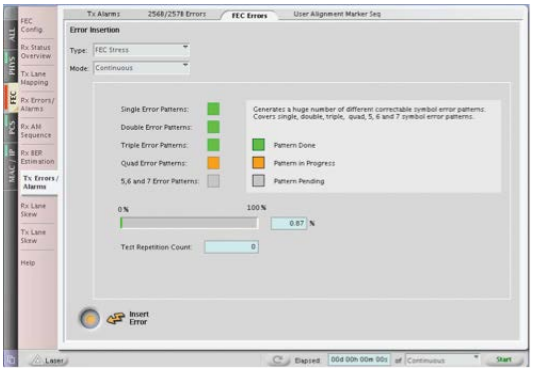
Graphical error/alarm matrix for all active flows with current and historical results. Results of particular flows are selectable.



QoS measurements per flow

QoS alarms	LPAC (loss of performance assessment capability, that is, test frame sync is not possible)
	NFTF (no flow test frame)
QoS errors	Lost, duplicated, misinserted, out-of- order frames
Evaluation (type dependent)	Count, rate, ratio, seconds
Throughput MAC/IP	Bandwidth, utilization in bps and %
Transfer delay	Min., max., average, variation (packet jitter)
Latency measurement resolution is 1 ns average and 10 ns per packet.	
BERT Measurements (single flow)	
BERT alarms	LPAC
BERT errors	Bit error
Evaluation (type dependent)	Count, rate, ratio, seconds Start/stop and user-defined intermediate
Service Disruption Measurements per Flow	
Graphical service disruption matrix for all active flows with "Threshold exceeded" and "Disruption" results. Results of particular flows are selectable.	
Disruption results are given for any disruption that occurs above the disruption time threshold.	
Port Disruption (non-flow selective) Flow Selective	
Disruption result	Longest
Disruption result	Shortest, longest, last
Impairment separation	5 to 2^{28}–1 frames
Type	Lost, duplication, out of order, misinsertion, time-out, link alarm
Disruption Counters	
Results	Total disruptions, disruptions exceeding threshold
Evaluation	Count, rate, seconds
Packet Jitter Analysis per Flow	
Packet jitter is usually caused by queuing and routing across or buffering in switched-transport networks. The final effect of high-packet jitter is the number of rejected packets.	
Instantaneous jitter is defined as the difference between packet spacing of the transmitter compared to packet spacing of the receiver. Instantaneous jitter is a measure of jitter dynamics.	
Instantaneous jitter	Current, peak, average, minimum in ns, hits in count values
Hit threshold editable	10 ns to 10 s

RFC 2544 Testing	
RFC 2544 addresses the need for service providers to perform QoS measurements in Ethernet and IP networks. Vendors are mandated to qualify the correct behavior of their IP/Ethernet equipment.	
The 40/100G ONT lets users perform fully automated RFC 2544 testing at 40 and/or 100GE rates, as applicable. In detail, it performs throughput, frame loss, round-trip delay and back-to-back (burstability) tests. The RFC 2544 is suitable for local and wide area networks (LAN and WAN) as well as OTN-mapped applications. All set up parameters for the four tests are editable on one page, and all the test results are also shown on one page.	
Results throughput	Table, graph, bar graph
Results frame loss	Table, graph
Results latency, back to back	Table
Online parameters shown during the measurement	Test, status, current frame length, remaining test time
Ethernet Options	
40G Ethernet BN 3061/94.51	
adds support of native 40GE Ethernet via QSFP+ port. Will also enable 2nd port if available	
Multistream/IP BN 3061/94.54	
adds IP and Multistream (up to 128 flows) support to available 100G or 40G Ethernet	
SR4 FEC Validation	
The advent of QSFP28 optical modules is driven by the deployment of SR4, CWDM4, and PSM4 datacom and telecom interfaces. In this environment, test equipment must evolve to accommodate this form factor into existing products to test and validate next-generation 100G interfaces.	
Deploying 25G I/O-based SR4 interfaces using multimode fiber requires overcoming the inter-symbol interference challenges that dispersion causes in the fiber from using lower-cost optics. One method for achieving this is using RS FEC (per IEEE 802.3bj Clause 91) to improve link performance and thus achieving the desired BER performance without adding to the optics and line cards cost.	



SR4 FEC Validation Option BN 3076/94.35	
Requires optional CFP2 to QSFP28 or CFP2 to CFP4 adapter	
Error insertion	
Supports simultaneous error and alarm insertion	
Type	Invalid transcoded block (ITB) and user-defined alignment marker sequence
Trigger	Once, continuous, burst once/ continuous
Burst	N events off, M events on
N, M	1 up to 2,147,483,647 events
Alarm insertion	
Simultaneous error and alarm insertion is supported	
Error evaluation	
Type	Uncorrectable code word, correctable code word, correctable symbol, correctable bit, correctable one bit, correctable zero bit, LOAMPS event, LOA event
Evaluation (depends on type)	Count, ratio, rate, seconds; summary; and per lane
Alarm evaluation	
Type	LOAMPS (summary, per lane), LOA (loss of alignment), and HI SER
Evaluation	Seconds
Lane alignment marker insertion	
For all virtual lanes	User-defined
SR4FEC lane mapping	
TX lane mapping	User-programmable (shift)
Lane skew generation	
Static skew per physical lane 0 to 64,000 bits	
Resolution	1 bit per physical lane

25G Ethernet Testing

25G Ethernet BN 3076/94.37	
PCS Configuration	
It is settable, if the PCS layer is operating according to IEEE Clause 107 or to 25G Ethernet Consortium (Schedule 3)	
64B/66B Error insertion	
Simultaneous error and alarm insertion is supported	
Type	Invalid sync header, User defined control block, Error propagation/E/
Trigger	Once, rate, burst once/cont.
Rate	9.9×10^{-3} to 1×10^{-10}
Burst	N events off, M events on
N, M	1 up to 1,073,741,823 events
Sync header value	Editable 0 to 3
User defined control block	8 bytes editable 0 to 255

64B/66B Alarm insertion	
Simultaneous error and alarm insertion is supported	
Type	LOBL (loss of block lock), HI BER [1] (High Bit Error Ratio)
Trigger	Continuous

1) According to IEEE Clause 107 or 25G Ethernet Consortium (Schedule 3)

Reconciliation Alarm insertion	
Simultaneous error and alarm insertion is supported	
Type	Local Fault, Remote Fault
Trigger	Continuous, burst once/cont.
Burst	N events off, M events on
N, M	4 up to 67,108,860 events (in steps of 4)

64B/66B Error evaluation	
Type	Invalid sync header, Errored block, Invalid block, LOBL events HI BER[1] events
Evaluation (depends on type)	count, ratio, rate

1) According to IEEE Clause 107 or 25G Ethernet Consortium (Schedule 3)

64B/66B Alarm evaluation	
Type	LOBL HI BER[1]
Evaluation	Seconds
Type	LOAMPS (loss of alignment marker payload sequence), HI SER (high symbol error rate)
Trigger (depends on type)	Continuous

Reconciliation Error evaluation	
Type	Error Propagation/E/, Local Fault events, Remote Fault events, IPG Violation events
Evaluation (depends on type)	count, ratio, rate

Reconciliation Alarm evaluation	
Type	Link Down, Local Fault, Remote Fault, IPG Violation
Evaluation	Seconds

25GE MAC Layer Specifications	
Please also refer to chapter "PCS and Ethernet Layers"	
Error Insertion	
Simultaneous error and alarm insertion is supported	
Type	Invalid Transcoded Block (ITB),User Defined Codeword Marker Sequence
Trigger	Once, continuous, burst once/cont.
Burst	N events off, M events on
N, M	1 up to 16,777,215 events
Type	Correctable Codeword Error, Uncorrectable Codeword Error, User Defined Symbol Error
Trigger	Once, continuous, sustained, burst once, burst cont.
Burst	N events off, M events on
N, M	1 up to 2,147,483,647 events
Alarm insertion	
Simultaneous error and alarm insertion is supported	
Type	LOCWMS (loss of codeword marker sequence), LOFECBL (loss of FEC block lock)
HI SER (high symbol error rate)	
Trigger (depends on type)	Continuous, Single Burst, Continuous Burst
25GE RS-FEC and BASE-R FEC (BN 3076/94.38)	
Adds optional RS-FEC and Base-R FEC support to available 25GE	
Function RX Description and details	
FEC Type TX/RX	· Bypass (FEC generation/evaluation is disabled) · Reed-Solomon FEC · BASE-R FEC
FEC/PCS	Mode
TX/RX	· IEEE 802.3 - Bypass: Clause 107 - RS FEC: Clause 108, Clause 107 - BASE-R FEC: Clause 74, Clause 107 · 25G Ethernet Consortium (Schedule 3)
FEC Bypass Correction	
RX Enable/disable FEC Bypass Correction.	
25GE FEC Validation (BN 3076/94.39)	
Adds in-depth 25GE FEC evaluation features, runs on one port only	
FEC Error Insertion:	
Type	Invalid Transcoded Block (ITB), User Defined Codeword Marker Sequence
Trigger	Once, continuous, burst once/cont.
Burst	N events off, M events on
N, M 1 up to 16,777,215 events	
Type	Correctable Codeword Error,Uncorrectable Codeword Error,User Defined Symbol Error
Trigger	Once, continuous, sustained, burst once, burst cont.
Burst	N events off, M events on
N, M 1 up to 2,147,483,647 events	
FEC Alarm Insertion	
Type	LOCWMS (loss of codeword marker sequence), LOFECBL (loss of FEC block lock),HI SER (high symbol error rate)
Trigger (depends on type)	Continuous, Single Burst,Continuous Burst

Error and alarm evaluation:	
Type	Uncorrectable codeword, Correctable codeword, Correctable symbol, Corr. Bit, Corr. One Bit, Corr Zero Bit, Corr. burst codeword, Corr. random error, Corr. burst bit, LOCWMS event, LOFECBL event
Evaluation (depends on type)	count, ratio, rate, seconds
Codeword Marker Insertion	user-defined codeword marker
Codeword shift/FEC block shift insertion	0 … 256 bits

50G Ethernet Testing

50GE (BN 3076/94.43)

Adds basic 50GE testing capabilities. Will run on port 1 only.
For details, see 25GE section

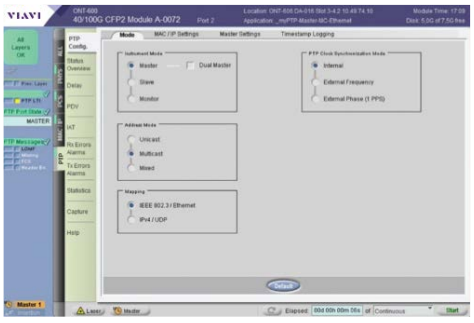
50GE FEC Validation (BN 3076/94.43)

Adds in-depth 50GE FEC testing capabilities. Will run on port 1 only.
For details see 25GE FEC Validation section.

IEEE 1588V2 PTP Master Slave Evaluation (BN 3061/94.84)

As mobile operators continue to deploy IEEE 1588v2 in their mobile backhaul networks using primarily 1GE links at this time with a short-term plan to upgrade to 10GE to address the continuously increasing demand for higher bandwidth, network equipment manufacturers and timing sources vendors must prepare for tomorrow's bandwidth challenges.

As 40GE/100GE technologies have matured and are ready for mainstream use, it has become evident that precision timing protocol (PTP) must be scaled to these bit rates on the aggregation side of the network. Now that grand master clocks are being designed with 40GE/100GE ports, these elements' performance must be thoroughly verified. The PTP evaluation option for ONT-600 100G CFP2 modules provides in-depth test capabilities for analyzing 100GE and 40GE system1588V2 PTP implementation.



Modes of Operation	
Emulation	Single master, dual master, slave clock
PTP Modes	1 and 2 step mode
Monitoring mode (listen only)	Monitor traffic from Master to Slave, Slave to Master
PTP Packet Generation	
Packet rate	1/256 …. 256 packages per second
PTP Analysis	
Modes	packet delay, packet delay variation, delay asymmetry, packet inter arrival time
Time stamp logging	T1, T2, T3, T4 and correction fields, 5 ns resolution
Number of log entries	up to 100E6, can be exported for offline analysis
Ethernet background traffic	
Traffic profile	up to 16 background flows with different traffic parameters
Errors and alarms	
RX Alarms	Loss of Message Flow (LOMF), Loss of Master Clock (LOMC), Loss of Timing Information (LTI) – resolution 1 s
RX Errors	FCS error, IP V.4 Header Error, Missing Message
Analysis modes	seconds (for alarms), count, ratio (for errors)
Error insertion types	dropped messages, runt messages, invalid start of frame delimiter, IP V4 header error
Message statistics	
Port states	disabled, listen, master, slave, monitor
TX and RX PTP message types	Signaling Announce, Sync, Follow-Up, Delay Response Delay Request (count, rate)
RX PTP messages	all, filtered in
Graphical result history	80 min for 2 message types, resolution 10 s
PTP packet capture	256 MByte (Wireshark format)

Modes of Operation	
Emulation	Single master, dual master, slave clock
PTP modes	1 and 2 step mode
Monitoring mode (listen only)	Monitor traffic from master to slave and slave to master
PTP Packet Generation	
Packet rate	1/256 … 256 packages per second
PTP Packet Generation	
Modes	Packet delay, packet delay variation, delay asymmetry, packet inter-arrival time
Time stamp logging	T1, T2, T3, T4 and correction fields, 5 ns resolution
Number of log entries	Up to 100E6, can be exported for offline analysis
Ethernet Background Traffic	
Traffic profile	Up to 16 background flows with different traffic parameters

Modes of Operation	
Errors and Alarms	
Rx alarms	Loss of message flow (LOMF), loss of master clock (LOMC), loss of timing information (LTI) – resolution 1 s
Rx errors	FCS error, IP V.4 header error, missing message
Analysis modes	Seconds (for alarms), count, and ratio (for errors)
Error insertion types	Dropped messages, runt messages, invalid start-of-frame delimiter, IP V4 header error
Message Statistics	
Port states	Disabled, listen, master, slave, monitor
Tx and Rx PTP message types	Signaling announce, sync, follow-up, delay response delay request (count, rate)
Rx PTP messages	All, filtered in
Graphical result history	80 min for 2 message types, resolution 10 s
PTP packet capture	256 MByte (Wireshark format)
Error evaluation	
Type	Uncorrectable codeword, Correctable codeword, Correctable symbol, Corr. Bit, Corr. One Bit, Corr. Zero bit, Corr. burst codeword, Corr. random error, Corr. burst bit, LOCWMS event, LOFECBL event
Evaluation (depends on type)	Count, ratio, rate, seconds
Alarm evaluation	
Type	LOCWMS, LOFECBL, HI SER
Evaluation	Seconds
Codeword marker insertion	
Codeword marker	User-defined
Codeword shift/FEC Block shift insertion	
Shift	0 to 256 bits

Modes of Operation
Emulation: Single master, dual master, slave clock
PTP modes: 1 and 2 step mode
Monitoring mode (listen only): Monitor traffic from master to slave and slave to master
Synchronization
Internal, from ONT clock module (1 pps external clock)
Selectable Addressing Modes
Multicast Unicast
Transport Layer
Ethernet MAC, VLAN (up to 2 tags), SNAP, IPv4
Ethernet Background Traffic
PTP Packet Generation
Packet rate: 1/256 – 256 packets per second

Modes of Operation	
Packet types	Announce, sync, delay request, delay response
PTP Time Stamp Evaluation	
Types	Packet delay, packet delay variation, delay asymmetry, packet inter-arrival time
Time stamp logging (master)	T1, T3, T4 including correction field
Time stamp logging (slave)	T1, T2, T2a, T3, T4, T5 including correction field
Number of log entries	Up to 100 million time stamps
Time stamp post processing	Via wander analysis software (BN 3061/95.98 and 3061/95.99)
Time stamp resolution	1 ns
Error and Alarms	
RX alarms	Loss of message flow (LOMF), loss of master clock (LOMC), loss of timing information (LTI) - resolution: 1 s
RX errors	FCS error, IPv4 header error, missing message
Result modes	Seconds (for alarms), count, ratio (for errors)
Error insertion types	Dropped messages, runt messages, invalid start of frame delimiter, IPv4 header error
Message Statistics	
Port states	Disabled, listen, master, slave, monitor
TX and RX PTP message types	Signaling, announce, sync, follow-up, delay response, delay request (count, rate)
RX PTP messages	All, filtered in
Graphical result history	> 1 hour for 2 message types, resolution: 10 s
PTP packet capture	256 MB (Wireshark format)

External Wander Analysis Software

External Wander Analysis (Option BN 3061/95.98) **Packet Data Add-On for Wander Analysis (Option BN 3061/95.99)**
In-depth Windows-based analysis tools for logged time-stamp data; comparison of data against all relevant masks per ITU-T G.826x, 827x and others
Sychronous Ethernet
SyncE G.8264 ESMC Testing (BN 3076/94.89)
Synchronous Ethernet (SyncE) equipment requires clock-quality reporting capabilities, and as specified in recommendation ITU-T G.8264 the Ethernet synchronization messaging channel (ESMC) provides these reporting capabilities by means of the synchronization status message (SSM) protocol.

SSM Generator	
All static settings of the transmitted SSM frames are displayed. The source address used for the SSM frame is equal to the MAC port address.	
SSM Insertion	On/off
Send mode	Single frame, continuous
Message rate	0.1 to 20.0 fps
QL mode	Static, alternating
QL duration	1.0 to 3,600.0 s
SSM asynchronous event	On/off
SSM Analyzer	
SSM timeout threshold	1 to 60 s
Sliding window size	1 to 10 s
SSM status display	SSM timeout, SSM rate, last Q-code
SSM statistics	Average/peak rate, min/max inter-frame gap
SSM Delay Measurement:	
Switching delays of synchronous Ethernet equipment can be measured by triggering a change of the reported clock quality of an incoming link and simultaneously monitoring the change of reported clock quality of an outgoing link. Through a flexible trigger mechanism, a delay measurement is started when a user-defined trigger match is detected and stopped when the corresponding RX trigger match is detected.	
Delay measurement	On/off
TX/RX trigger conditions	Any QL change, Rising QL, Falling QL, Change to QL
Delay measurement	resolution ms
Display of all results with time stamps	
Criteria	Start, end, duration, count
Viewing filters	Events, durations, count
Graphical View	
Display of all events as bar graphs versus time. Cursors allow easy identification and zooming (in and out) on results.	
Viewing filters	Events
Time axis scale	Second, minute, hour

OTN

OTL Layer	
40G OTL3.4 and 100G OTL4.4	
Highlights	
OTL3.4 and OTL4.4 BERT	

- Sophisticated OTL-layer testing with skew measurements
- Dynamic skew generation (optional)
- Support of lambda groups
- Real-time analysis per logical lane

OTL Layer	
Basic Features	
Payload of OTL Frames	
PRBS pattern PRBS9, -23, -31 and inverted	
OTL Alarm Generation	
Alarm types	LOFOTL, OOFOTL
Mode	Continuous (into all lanes, into selected lane)
OTL Error Insertion	
OTL4 error types	FAS, LLM, MFAS, user-defined LLM, user- defined MFAS
OTL3 error types	FAS, MFAS, user-defined MFAS
Mode	Once, rate, burst once, burst cont. (into all lanes, into selected lane)
Rate	9.9×10^{-3} to 1.0×10^{-10}
Burst	M errored, N non-errored frames
M, N	1 to 16,777,215
Mode	Invert, overwrite
LLM value	0 to 255
LLM mask	0 to 255
MFAS value	0 to 255
MFAS mask	0 to 255
Payload Error Insertion	
Error type	Bit error
Triggering	Once, rate
Rate	1.0×10^{-2} to 1.0×10^{-10}
Lane Mapping	
TX lane mapper allows lane rotation at assigned OTL lane.	
Static Skew Generation	
Range	0 to 64,000 bits
Dynamic Skew Generation	
Mode	Manual, triangle
Skew (manual)	–32,000 to 32,000 in mUI
Latest peak (triangle)	–32,000 to 32,000 in mUI
Earliest peak (triangle)	–32,000 to 32,000 in mUI
Slope	10, 20, 50, 100, 200, 500, 1,000 mUI/s
Applied lane	Any physical lane
OTL4.4 Lambda Group Configuration	
Number of groups	4
Mode	Manual, apply per alarm lane
Total Analysis (aggregate)	
Graphical error/alarm matrix for all logical lanes with current and historical results.	

User-Defined Error Insertion	
OTL3.4 Measurements	
OTL alarms	LOFOTL, OOFOTL, LOR, OOR, OOMFAS, LOL, OOL, LL swap
OTL errors	FAS, MFAS
Evaluation (type dependent)	Count, ratio, seconds
OTL4.4 Measurements	
OTL alarms	LOFOTL, OOFOTL, LOR, OOR, OOLLM, OOMFAS, LOL, OOL, LL Swap
OTL errors	FAS, LLM, MFAS
Evaluation (type dependent)	Count, ratio, seconds
Maximum Skew	
Evaluation	Current max. skew in bits and picoseconds between earliest and latest lane
Analysis per Logical Lane	
Lane ID	
Evaluation	Current lane ID
OTL3.4 Measurements per Logical Lane	
Graphical error/alarm matrix for all logical lanes with current and historical results. Results of particular lanes are selectable. Alarms/ errors are shown in a common table.	
OTL alarms	LOFOTL, OOFOTL, LOR, OOR, OOMFAS
OTL errors	FAS, MFAS
Evaluation (type dependent)	Count, ratio, seconds
OTL4.4 Measurements per Logical Lane	
Graphical error/alarm matrix for all logical lanes with current and historical results. Results of particular lanes are selectable. Alarms/ errors are shown in a common table.	
OTL alarms	LOFOTL, OOFOTL, LOR, OOR, OOLLM, OOMFAS
OTL errors	FAS, LLM, MFAS
Evaluation (type dependent)	Count, ratio, seconds
Logical Lane Skew (delay)	
Evaluation	Current skew (in bits and picoseconds)
Analysis per Lambda Group	
OTL3.4 Measurements per Lambda Group	
Alarms	LOFOTL, OOFOTL, LOR, OOR, OOLLM, OOMFAS
Errors	FAS, MFAS
Evaluation (type dependent)	Count, ratio, seconds

OTL4.4 Measurements per Lambda Group	
Alarms	LOFOTL, OOFOTL, LOR, OOR, OOMFAS
Errors	FAS, LLM, MFAS
Evaluation (type dependent)	Count, ratio, seconds
Payload Measurements (aggregate)	
Payload alarms	Pattern loss
Payload errors	Bit error, errored one, errored zero
Evaluation (type dependent)	Count, ratio, seconds

OTU3 and OTU4 Testing Modes
Terminate Mode
Generators and analyzers run at the same OTN rate
Through Mode

Supports both intrusive and non-intrusive through mode. The generator and analyzer run at the same OTN rate and received traffic is terminated at the OTN layer and retransmitted with the transmitter. All OTN layer information remains unchanged in non-intrusive through mode, whereas intrusive through mode allows for it to be selectively overwritten with the OTN generator. The client signal remains unchanged and is retransmitted and analyzed by the higher layer, if supported.

- Standard and overclocked (optional) OTU3 and OTU4 rates
- Support of all TCM layers
- Transfer delay and service disruption
- Unique FEC stress testing with walking pattern
- Overhead byte capture
- 4-byte APS/PCC access

The functionality includes OTN framing as per G.709 with standard and/or overclocked rates.The OTN applications support generation and analysis of OH bytes, errors, alarms, and FEC. Parameters and measurement results at the OTN and client layer are processed simultaneously.

OTN Generator	
Pattern	OTN test, higher layer test, and live traffic
OTN test pattern	PRBS7, -11,-15, -23,- 31 and inverted; 32 Bit DW.
Supports both stuffing and non-stuffing of payload bytes.	

Client Offset—Stuffing

Adjust the asynchronous client offset within the ±65 ppm range to allow manipulation of the stuffing rate of the client.

Client stuffing generation (GMP): displays nominal and effective Cm value

Overhead (frame alignment/OTU/ODU/OPU)

All bytes are statically programmable except for MFAS, SM BIP, PM BIP, and TCM1 ... 6 BIP

- Additional possibilities for SM TTI, PM TTI, and TCM1 ... 6 TTI (trail trace identifier):
- Sequence consisting of the SAPI (16 bytes), DAPI (16 bytes), and the operator-specified (32 bytes)
- User-designed payload structure identifier (PSI), payload type identifier clear text, and MSI support
- One OH byte can be selected for a freely defined sequence of 16/32/64/128/256 bytes
- FTFL free definable forward/backward (FW/BW) fault indication and operator identifier
- 4-byte APS/PCC access

Error Insertion	
Type	FAS, MFAS, SM BIP-8, SM BEI, PM BIP-8, PM BEI, TCMi BIP-8, TCMi BEI (i = 1 to 6), OMFI, LOMFI, OOMFI applicable only with OTU4, bit errors (only available with OTN test pattern)
Trigger	Single, rate, burst, burst continuous
Burst error	M frames errors, N frames error free, M and N = 0 to 2^{31}

BIP Masks

The position and number of bit errors in the bytes can be selected. Valid for SM BIP, PM BIP, TCMi BIP (i = 1 to 6)

BEI Value

To stress the BEI evaluation of the DUT receiver the BEIs can be set to values from 0 to 15.

Valid for SM BEI, PM BEI, TCMi BEI (i = 1 to 6)

Alarm Generation

Type ODU-AIS, ODU-OCI, ODU-LCK, SM BDI, SM IAE, SM BIAE, PM-BDI, FW-SD, FW-SF, BW-SD, BW- SF, TCMi-LTC, TCMi-IAE, TCMi-BDI, TCMi-BIAE (i = 1 to 6), SM-TIM, PM-TIM, TCMi-TIM

Trigger	
Continuous	All alarms
Burst once/burst continuous	All alarms except LOS, LOF, TIMS, OOF, OOM, SD, SF
Burst alarms	M frames with alarm, N frames no alarm, M and N = 0 to 2^{31}

OTU FEC

The FEC generation can be switched on and off. Using the OTU FEC field, FEC based on the Reed-Solomon (255,239) algorithm is performed on the generated frame. Data blocks consisting of 239 data bytes and 16 FEC field bytes enable detection of up to 16 byte errors or correction of 8 byte errors.

FEC Error Insertion Modes

- FEC correctable, FEC uncorrectable
- FEC stress: This function allows for maximum stress tests within a short time frame. Inserts the maximum number of errors possible that the DUT can correct into the OTU frame by a walking pattern that affects all bit positions in less than 2 seconds.

FEC advanced

FEC advanced lets users define the position for error insertion in the OTU frame letting them perform correction capability testing below and above the correction limit.

Selectable parameters	Row, subrow, errored bytes per subrow, start position in subrow, byte error mask

OTN Analyzer

Client Stuffing

Displays payload offset in ppm.

Display of nominal and effective payload rate and Cm value.

Stuffing Counts

Positive, negative, sum count, duration of affected seconds.

Overhead Evaluation (frame alignment/OTU/ODU/OPU)

- Displays the complete overhead

SM TTI, PM TTI, TCM1 ... 6 TTI display of the 64 byte ASCII sequence of SAPI, DAPI, and Operator field

- Capture and display one sequence of up to 256 bytes for a selectable OH byte
- 4-byte APS/PCC access
- Displays payload structure identifier (PSI) bytes, payload type identifier (PT) clear text, and MSI support
- Editable PT expectation value as mismatch criterion
- FTFL forward/backward (FW/BW) fault indication and operator identifier fields

Trace References	
Set of SAPI and DAPI expectation values in traces SM TTI, PM TTI, TCM1 ... 6 TTI	
Select evaluation type of the received signal: SAPI or DAPI or SAPI/DAPI	
General Communication Channel Capture (GCC)	
The management information between the network element and the termination equipment is transported in the GCCs in the OTN overhead. This feature enables the capture of transmitted information in real time.	
Captured fields	GCC0, GCC1, GCC2, GCC1+2
Captured format	Raw
Capture size	up to 500 MB
Trigger	Manual
Error Measurement	
Validation of data for error measurement occurs after frame alignment, descrambling, and FEC computation and correction.	
Error Detection	
Types	FAS, MFAS, SM BIP, SM BEI, PM BIP, PM BEI, TCMi BIP, TCMi
BEI (i = 1 to 6), GMP CRC5/8, OMFI, bit error (only available for OTN test pattern), FECcorr. bit, FECcorr. code word, FECuncorr. code word	
Alarm Detection	
Type	LOF, OOF, LOM, OOM, OTU-AIS, ODU-AIS, ODU-OCI, ODU-LCK, SM BDI, SM IAE, SM, BIAE, SM-TIM, PM-BDI, PM-TIM, FW-SD, FW-SF, BW-SD, BW-SF, TCMi-LTC, TCMi-DI, TCMi-IAE, TCMi-BIAE, TCMi-TIM (i = 1 to 6), CSF, LOMF, OOMFI, CL-LOSS (client signal loss of synchronization), PT-MISM, pattern loss (only available for OTN test pattern)
Resolution	100 ms
Error and Alarm Results Display	
Numerical Display	
Displays count, ratio, and duration for each error	
Displays duration for each alarm	
Tabular Display	
Displays all results with time stamps	
Criteria	Start, stop, duration, count
Graphical Display	
Displays all events as bar graphs versus time. Cursors allow for easy identification and zooming (in and out) on results. Filters enable event selection.	
Time axis	Second, minute, hour
Live Traffic mode ignores pattern loss and bit errors allowing for analysis of live traffic without trouble indication.	

Service Disruption Test	
SD criteria	
Errors	MFAS, SM-BEI, PM-BIP, PM-BEI, bit errors
Alarms	LOS, LOM, OOM, SM-IAE, SM-BDI, SM-BIAE, ODU-AIS, ODU-OCI, ODU-LCK, PM-BDI
Event sample resolution	100 µs
Separation time	0.1 to 100,000 ms
Separation time starts at the end of the last event and is used to determine if the following event is a continuation of the same disruption (event occurs within separation time) or the start of the next one (event occurs after separation time has elapsed).	
Disruptions Results Display	
Numerical Display	
Total number of disruptions, begins with time stamp of first disruption and ends with a time stamp of last disruption.	
Shortest disruption time (with time stamp)	
Longest disruption time (with time stamp)	
Average Disruption Time	
Users can set service-disruption thresholds that range from 0 to 100,000 ms to identify when violations occur.	
Tabular Display	
Service disruption events with start/stop times and duration.	
Three logging modes are available (no logging; disruption events only; disruption and causing sensor events).	
Intermediate Bit Error	
In addition to the long-term bit error measurement, intermediate results are available.	
Interval	1 to 3,600 s
Results	Current/previous interval, count, and ratio

To analyze service disruption times, the ONT generates a high-speed event list as a result of all detected events.

Sensor to trigger service disruption test, selectable: sequence of SAPI, DAPI, and Operator field

- Capture and display one sequence of up to 256 bytes for selectable OH byte
- 4-byte APS/PCC access
- Displays payload structure identifier (PSI) bytes, payload type identifier (PT) clear text, and MSI support
- Editable PT expectation value as mismatch criterion
- FTFL forward/backward (FW/BW) fault indication and operator identifier fields

OTN SW Options

OTU3 bulk (BN 3061/94.57)

OTU3 bulk option enables a bulk PRBS payload to be carried in an OPU3, ODU3, and into an OTU3 signal. Full monitoring and alarm and error injection at each layer, as appropriate. Applications for delay, TCM, and others.

OTU3e1 bulk (BN 3061/94.58)

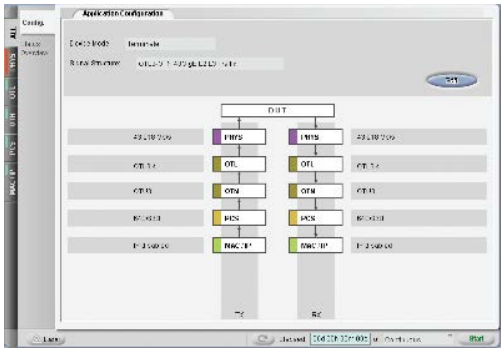
OTU3e1 bulk option enables a bulk PRBS payload to be carried in an OPU3e1, ODU3e1, and into an OTU3e1 (44.57 Gbps) signal. Full monitoring and alarm and error injection at each layer, as appropriate. Applications for delay, TCM, and others.

OTU3e2 bulk (BN 3061/94.59)

OTU3e2 bulk option enables a bulk PRBS payload to be carried in an OPU3e2, ODU3e2, and into an OTU3e2 (44.58 Gbps) signal. Full monitoring and alarm and error injection at each layer, as appropriate. Applications for delay, TCM, and others.

OTU3 with client (BN 3061/94.60)

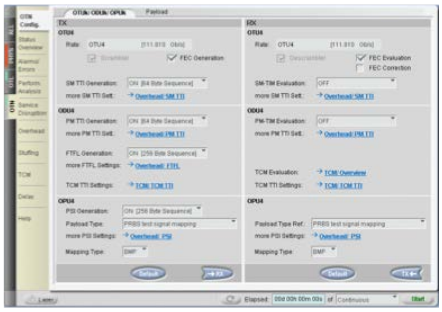
OTU3 with client enables a 40G Ethernet client transcoded into an OPU3, ODU3, and into OTU3. Full control of 40G Ethernet payload as well as monitoring and injection of alarms and errors as appropriate in each layer. Applications for TCM, delay, and service disruption, among others. Full monitoring and alarm and error injection at each layer, as appropriate.



Example of a 40GE client being transcoded into OTU3, fullcontrol of 40GE payload and all other layers to the physical layer are possible.

OTU4 bulk (BN 3061/94.55)

OTU4 bulk option enables a bulk PRBS payload to be carried in an OPU4, ODU4, and into an OTU4 signal. Full monitoring and alarm and error injection at each layer, as appropriate. Applications for delay, service disruption, and TCM, among others.



Example of OTU4 buld control screen

OTU4 with client (BN 3061/94.53)

OTU4 with client enables a 100G Ethernet client carried into an OPU4, ODU4, and into OTU4. Full control of 100G Ethernet payload as well as monitoring and injection of alarms and errors as appropriate in each layer. Applications for TCM, delay, and service disruption, among others. Full monitoring and alarm and error injection at each layer, as appropriate.

OTN enhanced multiplexing (BN 3061/94.61)

OTN enhanced multiplexing enables one level of lower-order multiplexing into the OTU3 and OTU4 signal. An additional option is required for direct multiplexing of ODU3 into OTU4. Applications for TCM, delay, and service disruption, and others. Full monitoring and alarm and error injection at each layer, as appropriate.

OTN multistage multiplexing (BN 3061/94.62)

OTN multistage multiplexing allows for multiple levels of multiplexing into the OTU3 and OTU4 (for example, ODU1 into ODU2 into OTU3) and applications for TCM, delay, and service disruption, and others. Full monitoring and alarm and error injection at each layer, as appropriate.

ODU0 bulk (BN 3061/94.63)

Enables the use of an ODU0 client with PRBS payload in the above multiplexing schemes.

ODUflex bulk (BN 3061/94.64)

Enables the use of an ODUflex client with PRBS payload in the above multiplexing schemes.

ODU0 with SDH/SONET client (BN 3061/94.65)

This feature maps an STM-1/STS3 or STM-4/STS12 signal into an available ODU0

ODU1/2 with SDH/SONET client (BN 3061/94.66)

This feature maps a 2.5 G SDH/SONET client into OPU1/ODU1 and a 10G SDH/SONET client into OPU2/ODU2 for further multiplexing into the outgoing OTU3 or OTU4 signal. It also provides simultaneous

ODU and SDH/SONET testing. To simulate real-world traffic, it supports GMP stuffing of an SDH/SONET client in the transmit direction and receive direction measurements.

OTN 10G Ethernet client mapping (BN 3061/94.68)

This option generates a 10G Ethernet signal used to map 10GBase-R traffic into ODU2e for multiplexing into OTU3, OTU3e1, OTU3e2, and OTU4 signals, depending on the instrument setup, and preserves 64B/66B line codes. It is also required for GFP-F mapping of MAC/IP into ODU1 or ODU2.

GFP-F up to 10G (BN 3061/94.77)

This option provides GFP-F test capability up to 10G. It can work with a 1 GE client (3061/94.70) to test GE with GFP-F into ODU0, and a 10GE client (3061/94.68) to test MAC/IP with GFP-F into ODU1, and MAC/IP with GFP-F into ODU2.

GFP-F up to 43G (BN 3061/94.67)

This option provides GFP-F test capability up to 43 G. It can work with a 1 GE client (3061/94.70) to test GE with GFP-F into ODU0, a 10GE client (3061/94.68) to test MAC/IP with GFP-F into ODU2, and a 43GE client (3061/94.51) GFP-F mapped into ODU3.

OTN GFP-F up to 100G (BN 3061/94.78)

This option provides GFP-F test capability (up to 100G), It can work with a 100GE client, GFP-F mapped into ODU4 or lower rate ODUs. Works in single port mode only, does not include GMP mapped 100GE into OTU4 (3061/94.53).

Transparent 10GE GFP-F mapping (BN 3061/94.69)

This option allows to map a PCS transparent 10G Ethernet signal into an available ODU2, using the Generic Framing Procedure/Framed (GFP-F). This method is also known as "AMCC mapping". Requires at least 10G GFP-F support (BN 3061/94.77).

1GE client (BN 3061/94.70)

This option enables GigabitEthernet as a client to ODU0 via the Generaric Framing Procedure – Transparent (GFP-T). The ODU0 bulk option and appropriate muxing structures are required.

The GE client also can be mapped into ODU0 via GFP-F when one of these GFP-F options is available: 3061/94.77 (GFP-F up to 10G), 3061/94.67 (GFP-F up to 40G), or 3061/94.78 (GFP-F up to 100G).

40G SDH/SONET

Adds full 40G SDH/SONET functionality and STL-256 BERT line rate will work in single and dual port mode.

For details on the capabilities of SDH/SONET, please see the generic SDH/SONET layer description. Can be combined with 3061/94.76.

SDH/SONET client in ODU3/OTU3 (BN 3061/94.76)

40G SDH/SONET mapping into into ODU3/OTU3.
Full testing access to SDH/SONET and OTN features

OTN control plane enhancement (BN 3061/94.81)

This option enables capturing and transmitting HDLC traffic in the OTU3 or OTU4 GCC channels (GCC0, GCC1, GCC2, or GCC1+2).

In addition, enables full MFAS synchronous access to the OTU overhead bytes, and allows drop & insert of external GCC traffic

OTN Enhanced Overhead Manipulation (BN 3076/94.87)

This option adds powerful additional capabilities to manipulate and overwrite the internally generated or passed-through TX OTU/OPU/ODU overhead of the OTN Layer. It is fully additional to the existing static Overhead, TTI, alarm & error insertions. Already available error/alarm insertion features may be used in parallel.

This adds a broad range of capabilities, such as (but not limited to): SAPI/DAPI trace errors and replacements; additional insertion of errors/alarms in parallel to the main error/alarm insertion.

It allows to test specific alarm/error transitions, e.g. in the GCC channels, the OSMC channel or the MFAS. Allows JC-byte manipulation (to test specific GMP mapping-errors). Up to 4 different Overhead bytes can be manipulated concurrently in single, M in N or repetitive modes, using flexible bit masks.

ODU Multichannel (BN 3061/94.73)

The OTN multichannel option enables in-depth, parallel analysis of up to 32 individual channels (ODU0) in an OTU3 or OTU4, depending on enabled options. This powerful analysis application helps end users develop, troubleshoot, and validate complex OTN applications, such as cross-connects.

Users can build signal structures and select a wide range of channel types, such as ODU0s through ODUflex to ODU2e, with a fully monitored and generated bandwidth up to 40G. Each channel has comprehensive high-resolution monitoring to fully control alarm and error generation.

10x10G ODU Multichannel (BN 3076/94.92)

The OTN multichannel option enables in-depth, full bandwidth parallel analysis of up to 10 individual channels (ODU2) in an OTU3 or OTU4, depending on enabled options. This powerful analysis application helps end users develop, troubleshoot, and validate complex OTN applications, such as cross-connects.

Each channel has comprehensive high-resolution monitoring to fully control alarm and error generation. Options 94.73 and 94.92 can be combined to achieve full bandwidth multi-channel test capabilities in a mixed mapping environment.

SDH/SONET client in ODU3/OTU3 (BN 3061/94.76)

Available 40G SDH/SONET can be mapped into ODU3/OTU3 structure. Full testing access to SDH/SONET and OTN features

40GE transcoded in ODU3/OTU4 (BN 3061/94.80)

Mapping of a transcoded 40G Ethernet signal into ODU3/OTU4

OTN Multistage Muxing via ODU3-OTU4 (BN 3061/94.82)

Mapping of lower rate ODU containers into ODU3-OTU4

100G MPLS/IP Client into OTN (BN 3061/94.83)

MPLS/P 100G client can be mapped into OTU4 via GFP-F (requires 94.78)

100G Ethernet D&I from ODU4/OTU4 (BN 3061/94.90)

Dual port option: allows to drop a 100G Ethernet signal from an OTU4, and to insert an external 100GE signal into an OTU4control alarm and error generation. Options 94.73 and 94.92 can be combined to achieve full bandwidth multi-channel test capabilities in a mixed mapping environment.

List of available OTN Stacks

The OTN features on the 40/100G platform have considerable breadth and depth, the range of options lets users scale applications to meet their needs.

Some of the optional applications depend upon other options being installed, most of the stacks will run on both ports of the CFP2 Module. The following table shows available stacks for dual port and single port modes. If in doubt please consult your VIAVI representative.

List of available OTN mappings. See order information section for details on options needed
OTL3-BERT, OTL3-OTN-BERT
OTL3-OTN-LAN-40GigE
OTL3-OTN-GFPF Ethernet *)
OTL3-OTN-ODU-BERT
OTL3-OTN-ODU-ODUflex BERT
OTL3-OTN-ODU-Multichannel BERT *)
OTL3-OTN-ODU2e-10GigE
OTL3-OTN-ODU0-GFPT 1GigE
OTL3-OTN-ODU-GFPF Ethernet
OTL3-OTN-ODU2-GFPF PCS Ethernet
OTL3-OTN-ODU-ODUflex GFPF Ethernet
OTL3-OTN-ODU-SONET/SDH BERT
OTL3-OTN-ODU-ODU BERT
OTL3-OTN-ODU-ODU0-GFPT 1GigE
OTL3-OTN-ODU-ODU-GFPF Ethernet
OTL3-OTN-ODU-ODU-SONET/SDH BERT
OTL3-OTN-ODU2-ODU1-ODU0 BERT
OTL3-OTN-ODU2-ODU1-ODU0-GFPT 1GigE
OTL3-OTN-ODU2-ODU1-ODU0-GFPF Ethernet
OTL3-OTN-ODU2-ODU1-ODU0-SONET/SDH BERT
OTL3-OTN-SONET/SDH BERT
OTL4-BERT, OTL4-OTN BERT
OTL4-OTN-100GigE
OTL4-OTN-GFPF Ethernet *)
OTL4-OTN-ODU-BERT
OTL4-OTN-ODU-ODUflex BERT
OTL4-OTN-ODU-Multichannel BERT [40G or 100G Bandwidth] *)
OTL4-OTN-ODU2e-10GigE
OTL4-OTN-ODU0-GFPT 1GigE
OTL4-OTN-ODU-GFPF Ethernet
OTL4-OTN-ODU2-GFPF PCS Ethernet
OTL4-OTN-ODU-ODUflex GFPF Ethernet *)
OTL4-OTN-ODU-SONET/SDH BERT
OTL4-OTN-ODU-ODU BERT
OTL4-OTN-ODU-ODU0-GFPT 1GigE
OTL4-OTN-ODU-ODU-GFPF Ethernet
OTL4-OTN-ODU-ODU-SONET/SDH BERT
OTL4-OTN-ODU2-ODU1-ODU0 BERT
OTL4-OTN-ODU2-ODU1-ODU0-GFPT 1GigE
OTL4-OTN-ODU2-ODU1-ODU0-GFPF Ethernet
OTL4-OTN-ODU2-ODU1-ODU0-SONET/SDH BERT
OTL4-OTN-ODU3 BERT
OTL4-OTN-ODU3-40GigE
OTL4-OTN-ODU3-GFPF Ethernet *)
OTL4-OTN-ODU3-SONET/SDH
OTL4-OTN-ODU3-ODU BERT
OTL4-OTN-ODU3-ODUflex BERT
OTL4-OTN-ODU3-ODU-SONET/SDH BERT
OTL4-OTN-ODU3-ODU-ODU BERT
OTL4-OTN-ODU3-ODU-ODU-SONET/SDH BERT
OTL4-OTN-ODU3-ODU2-ODU1-ODU0 BERT
OTL4-OTN-ODU3-ODU2-ODU1-ODU0-SONET/SDH BERT
40G SDH/SONET BERT

*) single port only

SDH/SONET Testing

Specification SDH Client
The specification describes the capabilities of the SDH/SONET layer for the native 40G STL-256 signal as well as for mapped SDH/SONET into the appropriate OTN structures, in particular: 40G STL-256 native 40G SDH/SONET (STM-256 or STS768) mapped into ODU3 STM-1/STS3, STM-4/STS-12 mapped into ODU0 STM-16/STS48 mapped into ODU1 STM-64/STS192 mapped into ODU2
Mappings
AU-3/VC-3, VC-4, VC-4-4c, VC-4-16c, VC-4-64c
Generation of Pointer actions · Pointer sequences with programmable spacing · Pointer increment/decrement (continuously repeated) · Single pointer · Pointer value setting with or without NDF · Offset simulation
Contents of SOH and POH bytes
The content of all bytes is programmable with any byte or a user defined byte-sequence p in m in n (p frames in m frames and the entire sequence repeated n times) can be inserted, with the exception of B- and H-Bytes.
SOH Capture
Single Byte and Double Byte
Capture depth: 512 value changes

Trace identifier	
J0, J1, J2	programmable 16/64 byte ASCII sequence with CRC
Error insertion and measurements	
Error types	B1, B2, B3 parity errors, FAS errors, MS-REI, HP-REI, bit errors in test pattern
Error Insertion Modes	
Single, Rate, Single Burst and Continuous Burst	
Alarm generation and measurements	
Alarm types	LOF, RS-TIM, MS-AIS, MS-RDI, AU-AIS, AU-LOP, HP-UNEQ, HP-PLM, HP-RDI, HP-RDI-C, HP-RDI-S, HP-RDI-P
Alarm Insertion Modes	Continuous, Single Burst and Continuous Burst
Test patterns and measurements	
PRBS11, -15, -23, -31 and inverted, 32 Bit DW	
Service disruption	
Number of disruption, first and last disruption, shortest and longest disruption	
Disruption Resolution 0.1 ms	

Specification SONET Client
Mappings
STS-1 SPE, STS-3c SPE, STS-12c SPE, STS-48c SPE, STS-192c SPE
Generation of Pointer actions · Pointer sequences with programmable spacing · Pointer increment/decrement (continuously repeated) · Single pointer · Pointer value setting with or without NDF · Offset simulation
Contents of TOH and POH bytes
The content of all bytes is programmable with any byte or a user defined byte-sequence p in min n (p frames in m frames and the entire sequence repeated n times) can be inserted, with the exception of B- and H-Bytes.
TOH Capture
Single Byte and Double Byte
Capture depth: 512 value changes

Trace identifier	
J0, J1, J2	programmable 16/64 byte ASCII sequence with CRC
Error insertion and measurements	
Error types	B1, B2, B3 parity errors, FAS errors, MS-REI, HP-REI, bit errors in test pattern
Error Insertion Modes	
Single, Rate, Single Burst and Continuous Burst	
Alarm generation and measurements	
Alarm types	LOF, TIM-S, AIS-L, RDI-L, AIS-P, LOP-P, UNEQ-P, PLM-P, RDI-P, RDI-P-C, RDI-P-S, RDI-P-P, PDI-P
Alarm Insertion Modes	Continuous, Single Burst and Continuous Burst
Test patterns and measurements	
PRBS11, -15, -23, -31 and inverted, 32 Bit DW	
Pointer generation	
Increment, Decrement, Sequence; Single, Periodic, Alternating	
Service disruption	
Number of disruption, first and last disruption, shortest and longest disruption	
Disruption Resolution 0.1 ms	

100G/40G CFP2 Based Modules and Options

Ordering Information

BN (Part#)	Description	Comments
	Modules	
3076/92.80	CFP2 100G/111G Phy/Data Single Port	CFP2 PHY single port module, includes native 100GE, can be upgraded to 40GE and OTU4 and physical layer options
3076/92.83	CFP2 100G/111G Phy/Data Dual Port	CFP2 PHY module with additional data port, includes native 100GE, can be upgraded to 40GE and OTU4 and physical layer options
	Software Options	
3076/94.31	CFP2 Advanced Error Analysis	Advanced bit error analysis, requires 94.30, runs on port 1 only
3076/94.32	CFP2 Dynamic Skew Variation	Inserts dynamic lane skew, requires 94.30, runs on port 1 only
3076/94.33	CFP2 Jittter Injection	Allows to insert jitter via electrical adapter, requires 94.30, runs on port 1 only
3076/94.34	CFP2 User Entered Bit rate 25 Gbps to 28 Gbps	Unframed testing at any rate from 25.3 to 28.05 Gbps, requires 94.30, runs on one or 2 ports
	Hardware Options/Accessories	
3076/92.90	CFP2 4x25G Electrical Adapter	Electrical access to 4x25 interface. Includes 4 times K1002. Will only work in Port 1 of ONT CFP2 Phy modules
K1001	Cable for External CFP2 MDIO Control	Needed to transfer MDIO signals to external eval board
K1002	Spare Cable assembly for CFP2 Electrical Adapter	8 coax cable assembly as spare for 3076/92.90
Dual Port Options (only available for 3076/92.83):		
	Software Options	
3061/94.90	100G Ethernet D&I from ODU4/OTU4	Requires 3076/92.81 or 83 or 3076/22 and 3061/94.53
3061/94.91	40G Ethernet D&I from ODU3/OTU3	Requires 3076/92.81 or 83 or 3076/22 and 3061/94.60
3076/94.40	100G/40G OTN Enhanced Muxing for 2nd Port	Requires 3061/94.61
3076/94.41	100G/40G Ethernet Client for 2nd port	Allows to have Ethernet client inside muxed structure on 2nd port (if available on 1st port); requires 3076/94.40 and at least one of 94.68, 69 or 70
3076/94.42	100G/40G SDH/Sonet Client for 2nd port	Allows to have SDH/SONET client inside muxed structure on 2nd port (if available on 1st port); requires 3076/94.40 and at least one of 94.65 or 66
3061/94.84	IEEE 1588 V2 PTP Master/Slave Evaluation	Will work on one or two ports; not available for ONT-602 (3076/22)
3061/95.98	External Wander Analysis	Windows SW for in-depth MTIE/TDEV/FFO/FFD analysis of imported TIE data from any ONT J/W card
3061/95.99	Packet Data Add-On for Wander Analysis	Adds IEEE 1588 based analysis of packet data to 3061/95.98
3076/94.30	CFP2 Hardware Validation	Allows static skew analysis and MDIO/I²C access (runs on port 1 only)
3076/94.35	SR4 FEC Validation	In-depth test and validation of SR4 FEC (runs on port 1 only. Basic SR4-FEC support available on 2 ports, no special option required)

BN (Part#)	Description	Comments
3076/94.36	MLG 1.0 Support	No prerequisites (runs on port 1 only)
3061/94.50	100G Ethernet	Adds 100GE to 3076/23, 24, 25, 26 or 3076/92.84, 85, 86 and 87 (single and dual)
3061/94.51	40G Ethernet	Adds 40GE to 92.8x, activates QSFP+ connector (single and dual)
3076/94.37	25G Ethernet	Adds basic 25GE functions (single and dual)
3076/94.38	25GE RS-FEC and Base-R FEC	Adds FEC support, requires 3076/94.37 (single and dual)
3076/94.39	25GE FEC Validation	Adds in-depth FEC evaluation features, requires 3076/94.38 (single and dual)
3076/94.43	50G Ethernet	Adds basic 50GE functions (runs on port 1 only)
3076/94.44	50GE FEC Validation	Adds in-depth FEC evaluation features, requires 3076/94.43 (runs on port 1 only)
3061/94.54	Multistream/IP	Adds IP and multistream (up to 256) capability (single port: full feature, limited # of flows in mapped dual port mode)
3076/94.89	ESMC G.8264	Generates and emulates ESMC SyncE messages
3061/94.55	111G OTN Bulk	Adds 111.8G OTU4 with bulk client (single and dual)
3061/94.57	100G/40G OTU3 bulk	Adds 43G OTU3 bulk to 94.51 (single and dual)
3061/94.58	100G/40G OTU3e1 bulk	Adds 44.57G OTU3e1 bulk (single and dual) to 94.57
3061/94.59	100G/40G OTU3e2 bulk	Adds 44.58G OTU3e2 bulk (single and dual) to 94.57
3061/94.61	100G/40G OTN Enhanced Multiplexing	Adds single stage multiplexing to 94.57 or 94.55, dual port needs 94.40
3061/94.62	100G/40G OTN Multistage Multiplexing	Adds multi stage multiplexing to 94.61 (not into ODU3 -> OTU4), dual port needs 94.40
3061/94.63	100G/40G OTN ODU0 bulk	Adds ODU0 with bulk to 94.61, dual port needs 94.40
3061/94.64	100G/40G OTN ODUflex bulk	Adds ODUflex with bulk to 94.61, dual port needs 94.40
3061/94.73	100G/40G OTN ODU Multichannel	Adds ODU Multichannel to 3061/94.55 or 94.57 (runs on port 1 only)
3076/94.92	100G/40G OTN 10x10G ODU Multichannel	Adds ODU Multichannel with full 10 x 10G bandwidth to 3061/94.55 (runs on port 1 only)
3061/94.81	100G/40G OTN Control Plane enhancements	Allows PPP D&I and analysis of payload HDLC frames in GCC bytes, requires 94.55 or 57 (runs on port 1 only)
3061/94.82	100G/40G OTN Multistage Muxing via ODU3-OTU4	Enables multistage muxing into ODU3-OTU4, requires 94.61 and 62, dual port needs 94.40
3076/94.87	100G/40G OTN Enhanced Overhead Manipulation	Fully flexible multiframe access to OTU Overhead bytes, requires 94.55 or 57, dual port needs 94.40
3076/94.88	100G/40G OTN OSMC Analysis	Adds capability to analyse OTN Synchronization Messaging Channel; requires 94.55 or 57, dual port needs 94.40

BN (Part#)	Description	Comments
3061/94.77	100G/40G OTN GFP-F up to 10G	Adds GFP-F mapped Ethernet functionality (up to 10G bandwidth), requires 94.55 or 57. Can be combined with 94.64 (ODUflex) and 94.61 (Muxing)
3061/94.67	100G/40G OTN GFP-F up to 43G	Adds GFP-F mapped Ethernet functionality (up to 43G bandwidth), requires 94.55 or 57, includes 94.77, can be combined with 94.64 (ODUflex). Port 1 only
3061/94.78	100G/40G OTN GFP-F up to 100G	Adds GFP-F mapped Ethernet functionality (up to 100G), requires 94.55, includes 94.67 and 94.77. Does not include 94.53. Port 1 only
3061/94.53	100G/40G OTU4 with Client	Adds capability to map 100G Ethernet via GMP into OTU4, requires 3061/94.55; will also run on 2nd port of 2 port modules
3061/94.60	100G/40G OTU3 with Client via transcoding	Adds capability to map 40G Ethernet/transcoded/requires 94.57, dual port needs 94.41
3061/94.80	100G/40G OTN 40GE transcoded in ODU3/OTU4	40GE transcoded Ethernet into ODU3/OTU4, requires 94.55, 61, dual port needs 94.40 and 41
3061/94.68	100G/40G OTN 10G Ethernet	Adds 10GE PCS mapped into ODU2e into available OTU3/OTU3e1/OTU3e2 or OTU4 , requires 94.55 or 57, and 61; dual port needs 94.40 and 41
3061/94.69	100G/40G OTN Transparent 10GE GFP-F mapped	Adds PCS transparent, GFP-F mapped 10G Ethernet (AMCC Mapping) into available ODU2, also requires 94.77; dual port needs 94.40 and 41
3061/94.70	100G/40G 1 GigE client	GigE via GFP-T into ODU0, requires 94.55 or 57, 61, and 63; dual port needs 94.40 and 41
3061/94.83	100G/40G OTN 100G MPLS/IP Client	Requires 94.78 (GFP-F) and 94.55 (OTU4 Bulk), runs on port 1 only
3061/94.72	40G SDH/SONET	Adds 40G SDH/SONET and STL-256 BERT line rate to 3061/94.51, both single and dual mode
3061/94.76	100G/40G OTN SDH/SONET client in ODU3/OTU3	40G SDH/SONET into ODU3/OTU3 , requires 94.57, dual port needs 94.40 and 42
3061/94.79	100G/40G OTN SDH/SONET client in ODU3/OTU4	40G SDH/SONET into ODU3/OTU4, requires 94.55, 61, 82; dual port needs 94.40 and 42
3061/94.65	100G/40G ODU0 with SDH/SONET Client	Adds SDH/SONET client in ODU0 to 94.63, dual port needs 94.40 and 42
3061/94.66	100G/40G ODU1/2 with SDH/SONET Client	Adds SDH/SONET client (concatenated or structured) in ODU1/2 to 94.61 or 94.62, dual port needs 94.40 and 42
Hardware Options/Accessories		
3076/92.92	CFP2 to CFP4; 4x25/28G; Passive Adapter	Allows to operate a 4 by 25/28G CFP4 transponder inside an ONT-600 CFP2 Module slot
3061/92.93	QSFP 40G LR4 Multi Rate Transponder	40G QSFP+ Transponder
3076/92.96	QSFP28 SR4 Multi Rate Transponder	SR4 Multi Rate Transponder, 850 nm Multimode, MPO
3076/92.98	CFP2 to SFP28 Active Adapter	Allows to operate an SFP28 transponder inside an ONT-600 CFP2 Module slot

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