



Three Steps to Overcome Signal Integrity Challenges

Overview

High-speed digital standards are quickly evolving to keep pace with the data demand from emerging technologies such as 5G, the Internet of Things, artificial intelligence, virtual reality, and autonomous vehicles. Each generational change of high-speed computing standards provides new signaling features, faster data transfer rates, and smaller design margins. Faster speeds create new design challenges that require higher-accuracy simulation, new software tools, and more efficient workflows.

The job of hardware engineers is to design, verify, build, and test electronic products. If they do not adopt new design methodologies, they risk product failure caused by the degradation of high-speed signals in the printed circuit board (PCB). Other risks include project delays, skyrocketing budgets, and possible career obstacles because their professional reputation is at risk. Engineers need new design tools and workflows to successfully design for the myriad interface standards, without increasing design and verification time.

Essential signal integrity analysis techniques include:

- eye diagrams
- mixed-mode S-parameters
- time domain reflectometry
- single-pulse response

Holistic Design Is Necessary as Complexity Increases

Signal integrity, the quality of an electronic signal, is all around us. In a digital communications channel, signal integrity analysis is the study of electrical signals as they traverse PCB traces, vias, connectors, and other components. Signal integrity problems can cause havoc for digital designs, resulting in performance issues, lower yield, and possible failures in the field. These problems can be costly because they often go undetected until late in the design and test cycle.

The best time to simulate a PCB for signal integrity is after layout and before fabrication. Taking the time to simulate the design becomes more critical as speeds increase. When speeds rise, a number of factors can lead to signal integrity problems, such as reflections at the interconnects (mismatched impedances), electromagnetic coupling between the traces, and grounding issues. If not addressed, these problems can cause signal distortion and attenuation.

Charting a Better Course Forward

Using signal integrity analysis and simulation is the best way to eliminate design problems prior to production. These techniques help save time and money by reducing the risk of late-stage design failures and maximizing design margin. Ideally, you need to consider signal integrity from the time you draw the schematic until the board passes the final test. Testing your assumptions with simulation is the best way to verify the signal integrity of your channel. To accomplish that, follow these three steps:

Step 1. Simulate the channel with an eye diagram

With a channel, transmitter, and receiver, the eye diagram can tell you how much the channel degrades the transmitted signal. The signal travels from a transmitter to a receiver across the PCB. Traces, connectors, and cables introduce interference that degrades a signal in both amplitude and timing. An eye diagram can help you determine if the quality of the signal is adequate when it reaches the receiver.

Figure 1 shows two different eye diagrams. The diagram on the left represents the signal at the transmitter side. The eye at the transmitter side is open; the digital 1 and 0 levels are clearly distinguishable. However, the eye closes after the signal goes through the channel and reaches the receiver. The receiver will have difficulty determining a digital 1 from a 0. The closed eye diagram identifies a signal integrity problem.

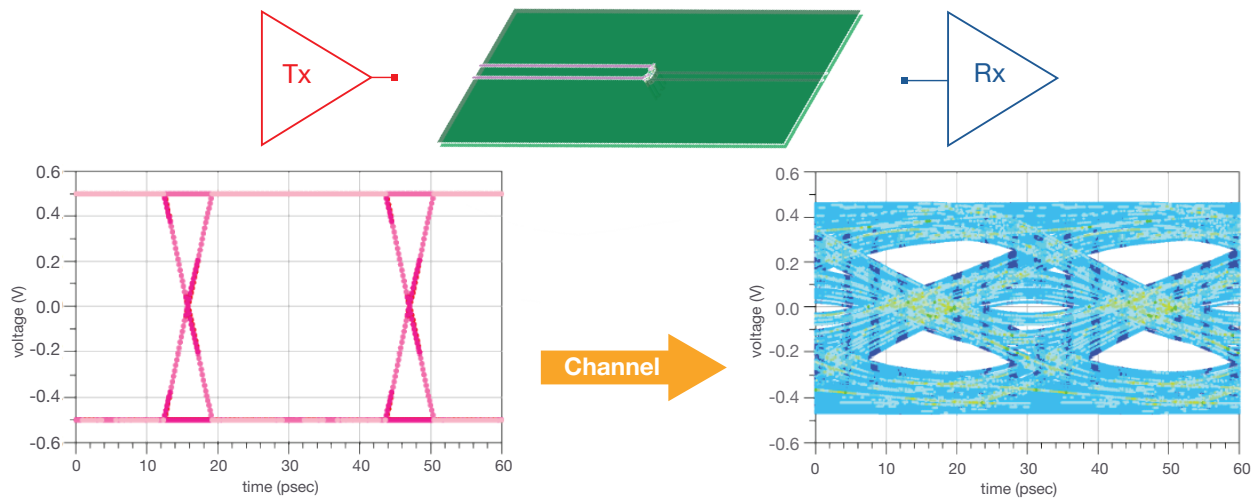


Figure 1. Eye diagrams provide a concise graphical representation of how a channel degrades the signal

Step 2. Locate the root cause of degradation

As it travels across the PCB, the signal can experience a substantial loss due to transmission lines. Once you discover a signal integrity problem, there are two primary analyses to determine the root cause of the problem in your design: mixed-mode S-parameters and time-domain reflectometry (TDR).

- **Mixed-mode S-parameters**

Use mixed-mode S-parameters to determine how the transmission lines react to differential and common signals from port 1 and port 2. Sending a sine wave with a frequency of f_0 at port 1, S_{11} reveals how much of the sine wave reflects from port 1.

Tables 1 and 2 depict how to interpret S-parameters.

S_{DD11}	Differential response at port 1 excited by differential input at port 1.
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Table 2. S_{DD} terms provide information about differential responses. S_{CD} terms indicate how much common signal is generated by differential input

S_{DD11}	Differential return loss
S_{DD21}	Differential insertion loss
S_{CD21}	Mode-conversion: EM generation
S_{DC21}	Mode-conversion: EM susceptibility

Table 2. S_{DD} terms provide information about differential responses. S_{CD} terms indicate how much common signal is generated by differential input

- **Time-Domain Reflectometry (TDR)**

As S-parameters tell you the frequency response of the channel, TDR provides the spatial and timing information. TDR uses reflected waveforms to give you the data on the channel (Figure 2). You can examine the single pulse response at the output by sending a single pulse with a specific rise time and data rate. To create the TDR plot, first express the channel impedance in terms of a known system reference impedance, Z_0 , and reflection coefficient, Γ . The reflection coefficient, Γ , is the ratio between the incident wave and the reflected wave. Once Γ is known, you can plot the impedance.

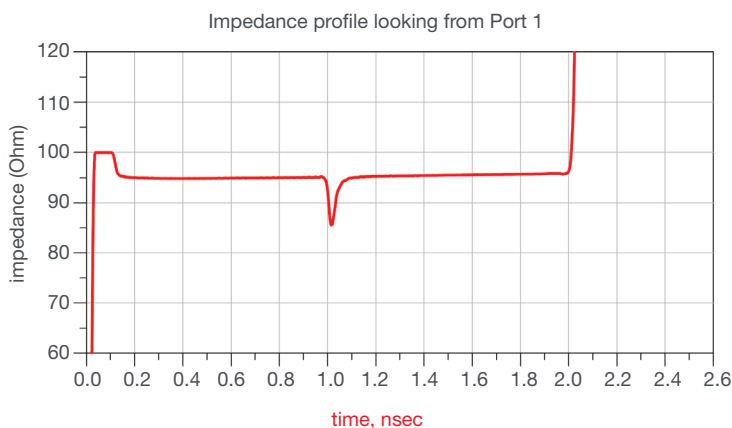


Figure 2. A dip at 1.0 nsec indicates a signal integrity problem in the channel

Step 3. Explore design solutions

Once you identify the root cause of the signal integrity problem, you need to consider what modifications you can make in your design.

One common cause of problems is the length of a via stub. A via is an electrical connection between layers in the PCB. The via stub is the unused portion of the connector that can significantly degrade signal quality. Back drilling is the process of removing the undesired stub section using a drill bit. It can provide significant improvements in signal integrity. After you make a design change, be sure to simulate the channel again to make sure your eye is open. Channel simulation enables rapid analysis of channels in high-speed serial and parallel communication links.

Once you finish exploring design solutions and simulate the channel to ensure signal integrity, you are one step closer to a successful high-speed digital design.

Overcoming Signal Integrity Issues

Tackling signal integrity issues in today's complex boards is challenging. Common challenges for signal integrity engineers include crosstalk, signal loss or distortion, and bandwidth degradation. You can identify the root cause of signal degradation using mixed-mode S-parameters and TDR. Engineers can avoid time and design challenges later on in product development by addressing signal integrity issues during the design stage.

For an in-depth look watch this video: [How to Solve Signal Integrity Problems: The Basics](#)

And for more information on how Keysight can help you overcome your signal integrity challenges, go to: www.keysight.com/find/pathwave