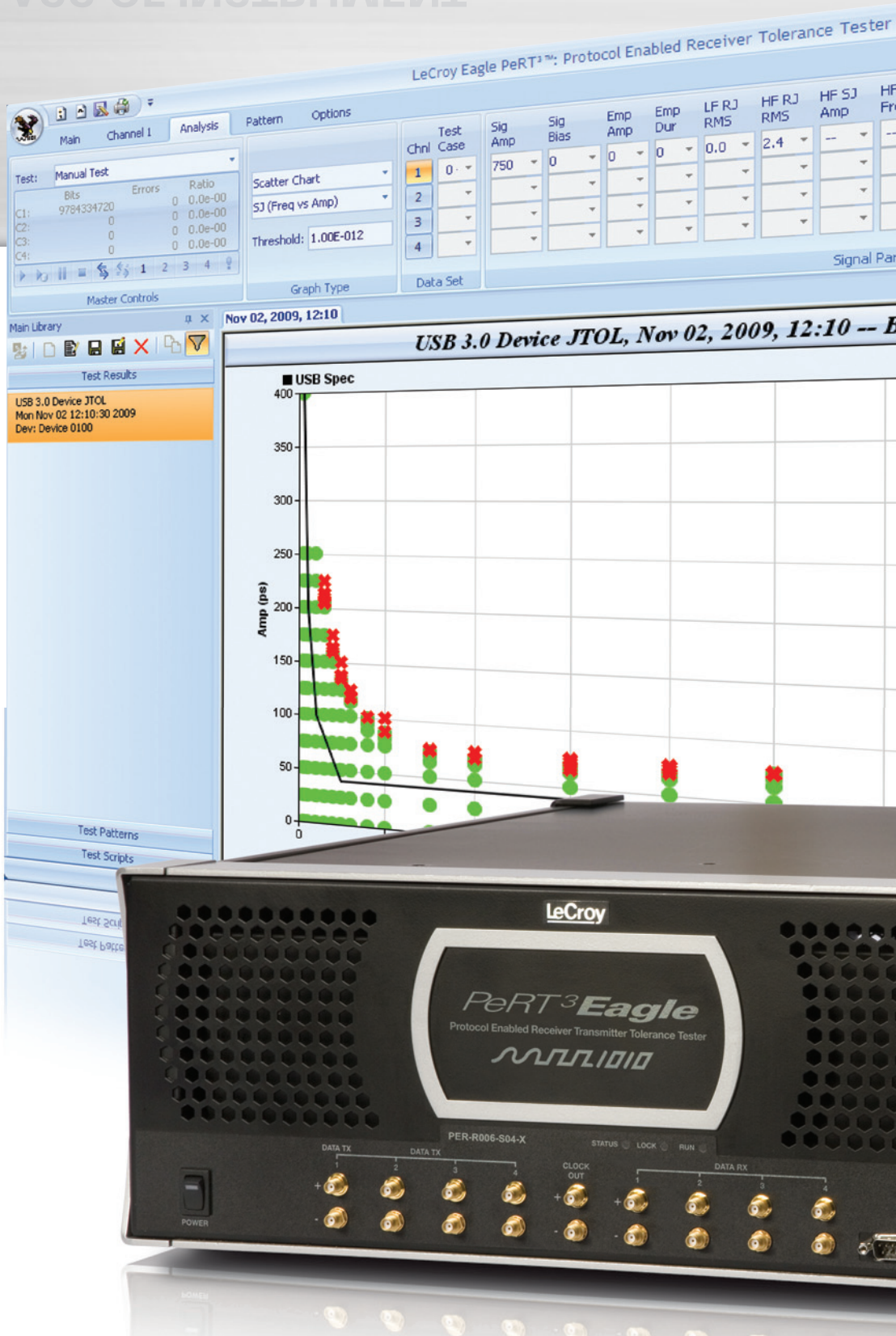
LeCroy

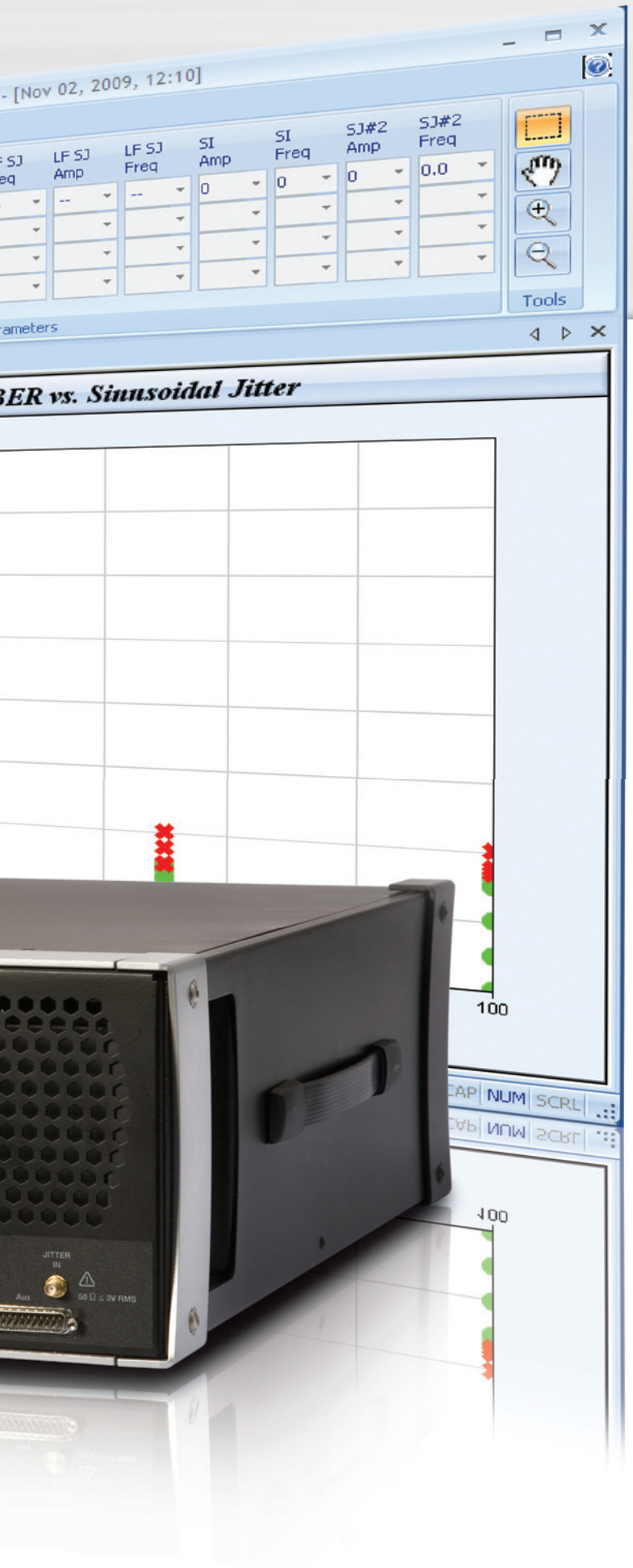
PeRT³™ Test System

Protocol-enabled Receiver and Transmitter Tolerance Tester

PeRT^3: A NEW CLASS OF INSTRUMENT

The PeRT^3 (Protocol-enabled Receiver and Transmitter Tolerance Tester) fills the space between physical layer test and protocol test, providing a new and more intelligent capability for performance testing of receivers and transmitters. Designed to meet the test needs of engineers working with serial data transceivers and other high-speed serial data communication systems, the LeCroy PeRT^3 Test System is not just a new instrument, it is an entirely new instrument class.



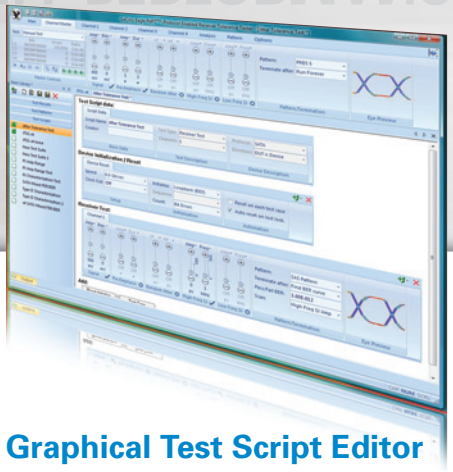


Key Features

- **BER Generator & Detector –** Up to 6 Gb/s high-speed pattern generator and error detector
- **Multichannel Operations –** Multichannel support up to 8 channels per system with independent jitter profile and analysis for each channel
- **Protocol Support –** Handshake, loop-back and FER support for PCI Express®, SATA, SAS and USB 3.0
- **Jitter Tolerance Testing –** Characterize and qualify high-speed serial transceivers
- **Integrated Pattern Generator –** Generates protocol level traffic using 1 GB user memory per channel with frames and data scrambling
- **Protocol Level Error Detection –** Recognizes and records protocol level errors such as ACKs, NAKs, and CRC errors
- **Stress Injection Capable –** Complete jitter profile including random (Rj), periodic (Pj), and sinusoidal (Sj)
- **SSC Support –** Enable or disable for silicon bring-up testing
- **Preemphasis –** 2 tap preemphasis with control of amplitude and duration
- **Input Sensitivity Testing –** Sweepable signal voltage for DUT input sensitivity test
- **Scripted Testing –** Automated test scripts allows for continuous testing for deep BER depth
- **Comprehensive Results –** Intelligent reporting capabilities for analysis and documentation of deep statistical tests
- **Support for Multiple Serial Data Standards –** Receiver compliance testing for PCI Express, SATA, SAS and USB 3.0

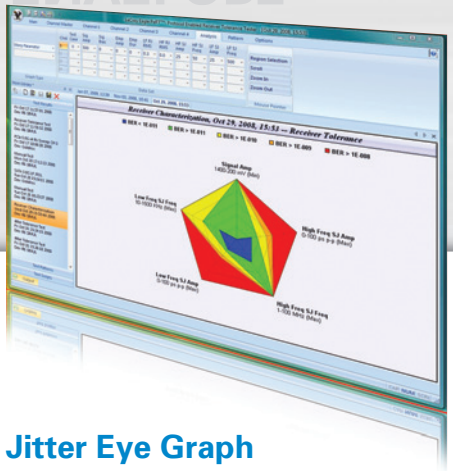
PERT^3: MAP THE FULL PERFORMANCE ENVELOPE

Developed through the synergy of LeCroy's electrical test and protocol test technologies, the PeRT^3 test system combines the functions and features of a signal generator, bit error rate tester (BERT), protocol editor and data analysis system in one instrument. This combination provides the ability to fully automate testing of transceivers and electronic systems in a comprehensive manner that not only measures adherence to specifications, but also examines the entire performance envelope of the system under test.



Graphical Test Script Editor

Simple, intuitive interface for creating automated test scripts. With a few clicks, set up automated tests that initialize the DUT and record error rates while sweeping through any user defined range of jitter parameters.



Jitter Eye Graph

A graphical description of device margins along multiple parameter axes. Provides an instant picture of margins vs requirements of the parameters you are interested in.

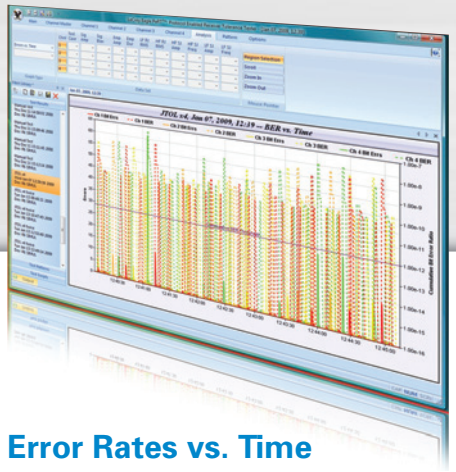
Complete Characterization in Development or Automated Test Environments

High-speed serial subsystem design and production is a sophisticated and delicate process of maintaining signal integrity from a transmitter that generates a signal passing through PCB traces, connectors and cables to a receiver at the other end. The process inevitably introduces deterioration in the signal in the form of increased jitter, electrical noise, reflections from connectors, amplitude fluctuations, timing distortions, and a host of other potential problems.

The design goal for the transmitter is to generate a strong, clean signal that can propagate through the channel and still deliver a quality signal at the other end. The design goal for the receiver is to be able to accurately decode weak signals with the accompanying noise and corruptions that occur in less than optimal connections. If both goals are accomplished, the result is a reliable and robust communications channel.

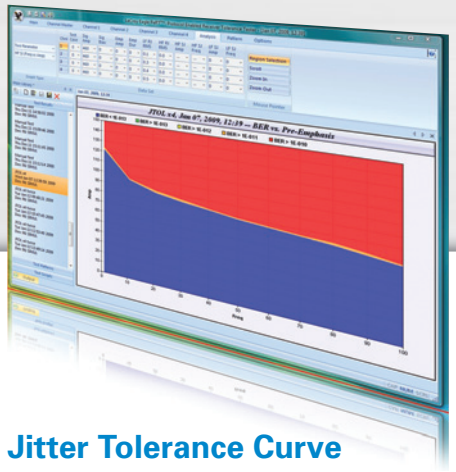
There is a set of specifications for each serial data standard (such as PCI Express, SAS, SATA, or USB 3.0) that is intended to ensure reliable signal transfer; at the electrical level through eye diagrams and bit error ratio testing, and at the protocol level through error detection schemes such as CRC.

Designers of serial transceivers, and users who are evaluating different designs from different vendors, need a more comprehensive test system that can explore the entire performance envelope of high-speed serial subsystem performance. Confirming that the device meets the industry specification is not always sufficient to distinguish between a device that barely passes the specification and a robust



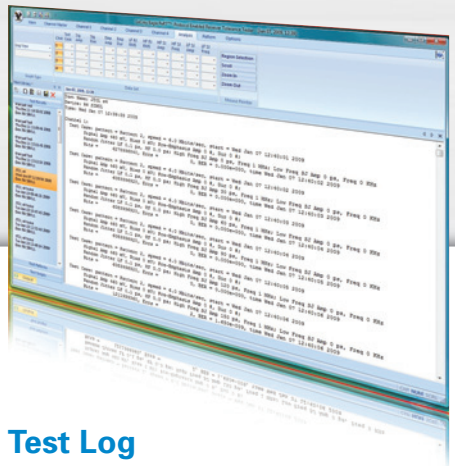
Error Rates vs. Time

Plot error rates as a function of time. Immediately see when errors occur.



Jitter Tolerance Curve

Plot error rates as a function of any two other parameters such as jitter amplitude and frequency. Identify device sensitivities to specific jitter frequencies. Verify the device tolerance against the specifications.



Test Log

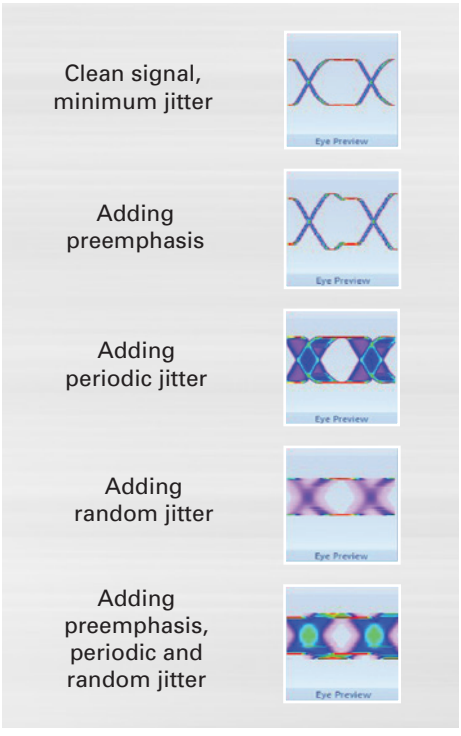
A full log of the stresses applied to the device under test and the resulting error rates, all logged against time.

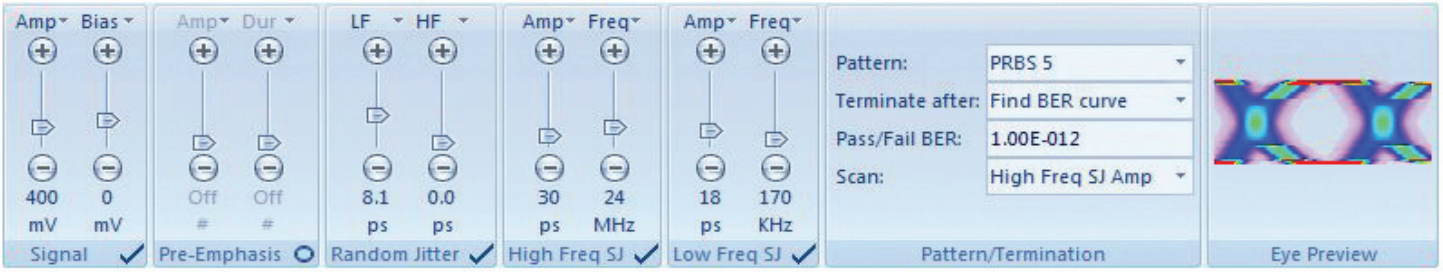
design that has significant margin to allow for real-world variations in conditions and signal quality.

Map the Full Performance Envelope Along Multiple Dimensions

Varying the type and amount of modulation introduced while counting the errors on the returning signal, the PeRT^3 maps out the full performance envelope of the device under test along multiple dimensions. This provides not just a GO/NO-GO test, but quantifies the error margins and error susceptibilities of each new design or each tested device. Should failure occur during the test, the environment that caused the failure can be generated by simply highlighting the report, and the design engineer has an environmental setup built to troubleshoot.

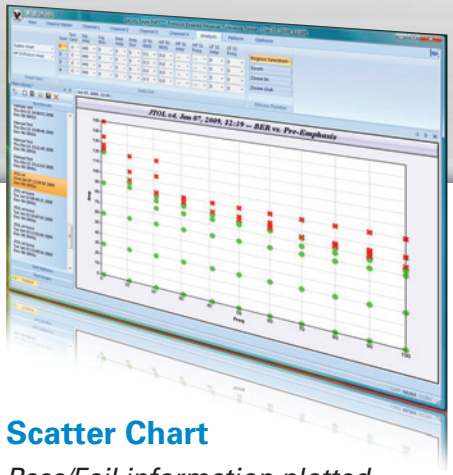
The PeRT^3 system is designed with simplicity in mind. Ready to use right out of the box, the PeRT^3 system provides easy exploration of the entire envelope of serial transceiver performance and more complete characterization of each design in either a development test or automated test environment.





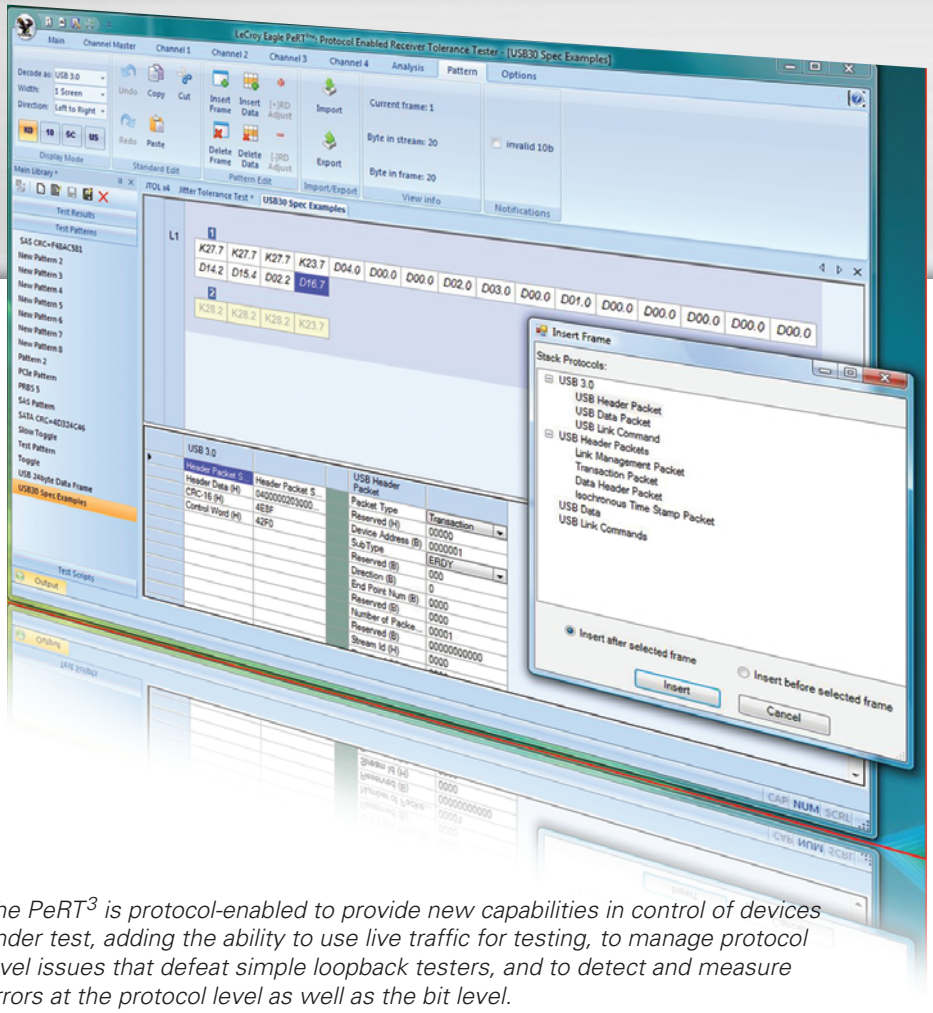
The PeRT^3 provides precise user control over signal and jitter generation, allowing rapid test development and comprehensive testing. As the user enters information, the resulting eye pattern is displayed in real-time.

PERT^3: PROTOCOL ENABLED



Scatter Chart

Pass/Fail information plotted against the stress parameters under test. See what happened for every test case—in real-time.



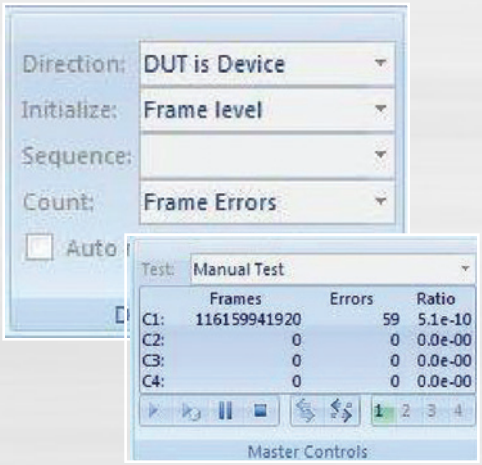
The PeRT^3 is protocol-enabled to provide new capabilities in control of devices under test, adding the ability to use live traffic for testing, to manage protocol level issues that defeat simple loopback testers, and to detect and measure errors at the protocol level as well as the bit level.

Protocol Enabled for Complete System Control, Real Data Traffic Generation, and Protocol Level Error Testing

Protocol enabling is a key advantage to using the PeRT^3 test system rather than other test instruments currently on the market. The PeRT^3 test system provides system control over the test configuration enabling automated testing. For example, the system can automatically command the remote device to enter a loop-back mode while a test is in progress.

The system can also generate test traffic that goes well beyond simple "pseudo random bit sequences" (PRBS) by using real data traffic. In addition, PeRT^3 intelligently manages protocol-specific issues that cause unnecessary disruptions, such as the resynchronization of clocks in SATA through the use of the ALIGN primitive.

Finally, the system can use protocol level error testing as one means for evaluating the system performance, measuring protocol-specific errors such as CRC errors, R_ERR in SATA or ACK/NAK in PCI Express.



By selecting Frame level initialization on the PeRT^3 main ribbon, you can send valid link level frames and directly count frames and frame errors while applying measured amounts of jitter—a capability unavailable in any other single tool on the market today.

SPECIFICATIONS AND ORDERING INFORMATION

Specifications

Generator Data Out

Bit Rate	1 to 6 Gb/s
Data Format	NRZ, normal or inverted
Rise/Fall Time (20–80%)	34 psec typical
Programmable Rise/Fall Time	Yes
Max. Rise/Fall Time Mismatch	0.05 UI
Differential Amplitude Range	50 mV to 1.8 V, 5 mV steps
Voltage Offset	-2.5 V to +2.5 V
Maximum AC Common Mode Voltage	20 mV
Maximum Intrinsic Jitter	< 20 psec typical
Tri-state Outputs	Yes
Electrical Idle Generation	Yes
SSC Support	Yes
Pre/De-emphasis Support	Yes
Return Loss SDD11 and S11	< -10 dB over entire frequency range

Generator Clock Out

Frequency Range	100 MHz to 6 GHz
Rise/Fall Time (20–80%)	34 psec typical
Voltage Rails	AC coupled
Jitter	1 psec RMS typical
Amplitude Range	CML
Sub-rate Clock	Divide by 1, or divide by any number between 8 and 511 (and multiplied by 1, 2, 4, or 8)
Jitter Stress	Yes

Protocols Supported

PCI Express	2.5 and 5 Gb/s
SAS	1.5, 3 and 6 Gb/s
SATA	1.5, 3 and 6 Gb/s
USB 3.0	5 Gb/s

Generator Jitter Stress

1.5 MHz – 100 MHz Rj (RMS)	12 psec
10 KHz – 1.5 MHz Rj (RMS)	12 psec
1.5 MHz – 100 MHz Dj P-P	240 psec
10 KHz – 1.5 MHz Dj P-P	240 psec
Periodic Jitter	Integrated and Calibrated
Sinusoidal Jitter	Integrated and Calibrated
Random Jitter	Integrated and Calibrated
Sine Interference	Integrated and Calibrated
Total Jitter	> 1 UI at high frequency, 10s of UIs at low frequency
External Jitter Injection	Yes

Error Detector Data In

Differential Amplitude Range	75 mV to 1 V
Format	NRZ

Ordering Information

Product Description	Product Code
PeRT³ Hardware Platforms	
Eagle PeRT³ System – 1 Channel	PER-R006-S01-X
Eagle PeRT³ System – 2 Channel	PER-R006-S02-X
Eagle PeRT³ System – 4 Channel	PER-R006-S04-X

Product Description	Product Code
Eagle Test Suite Options	
Eagle Jitter Tolerance Test Suite	PER-R006-008-A
Eagle SAS Receiver Test Suite	SAS-R006-004-A
Eagle SATA Receiver Test Suite	SAT-R006-004-A
Eagle PCI Express Receiver Test Suite	PCI-R006-008-A
Eagle USB 3.0 Receiver Test Suite	USB-R006-001-A

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Local sales offices are located throughout the world.
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