TELEDYNE LECROY
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PeRT³ Phoenix – Protocol Enabled Receiver and Transmitter Tolerance Tester

PROTOCOL AWARE BIT ERROR RATE TESTER

Key Features

- **Bit Error Rate tester with protocol aware capabilities**
- **Comprehensive jitter generation capability for receiver jitter and noise tolerance testing**
- **Built in 3 tap de-emphasis generator**
- **Protocol aware generator and receiver with 1 Gbyte space for custom patterns and protocol state machines**
- **10G option to enable full BER capabilities at 10Gbps**
- **Supports 128B/132B pattern generation and error detection**
- **Supports USB3.1 loopback initialization**
- **Complete jitter profile to support USB3.1 jitter tolerance testing at 10Gbps**
- **Built in De-emphasis generator**
- **SKP filtering and injections at 10Gbps**
- **User defined test scripting functions for jitter tolerance, equalization optimization search, and multi-parameter sweep testing**
- **User Customizable State Machines for protocol handshake and link training**

A New Approach for New Problems

In many new generations of high speed serial I/O standards, the protocol layer optimizes physical layer properties, such as optimizing equalization settings for accurate signal transmission to the receiver through long and noisy transmission mediums. This requires a PeRT^3 - a new class of instrumentation that can perform standard receiver tests and also communicate to the transmitter in protocol language. The PeRT^3 therefore ensures proper operation of integrated transmitter and receiver systems, optimizes test time, and minimizes equipment and setup complexity.

What is a PeRT^3?

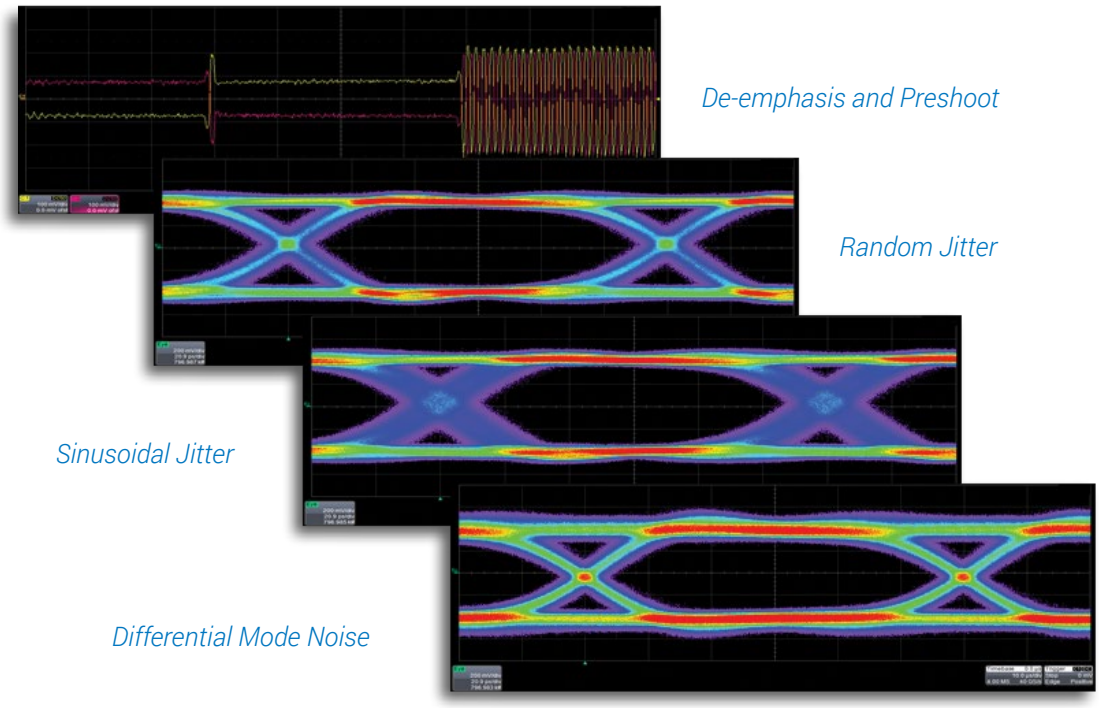
The PeRT3 (Protocol-enabled Receiver and Transmitter Tolerance Tester) fills the space between physical layer test and protocol test, providing a new and more intelligent capability for performance testing of receivers and transmitters. By having an instrument that is both a BER tester and a protocol emulator, the user can control the device under test (DUT) through protocol training while maintaining full jitter/noise injection and real-time equalization adjustments for BER measurements. This will help the user pinpoint issues hidden between the physical and protocol layer.

What is Protocol Awareness?

Protocol awareness is the ability to simulate and communicate real protocol traffic with the device under test. If the DUT is an end-point, the test equipment will simulate a system or root complex and vice-a-versa. PeRT3 contains built in state machines that perform various handshake protocols such as loopback initialization, equalization training and native frame error rate testing for PCI Express, USB 3.0, SATA and SAS. These features allows the user to test their product against standard compliance specifications as well as provide the foundation to troubleshoot complex signal integrity issues that may cross between the physical and protocol layer.

What are the Components of a PeRT3?

PeRT3 is fundamentally a BERT system which consists of a pattern generator and an error detector. The pattern generator has the ability to generate NRZ and out of band signals combined with a wide range of vertical and horizontal noise/jitter. At the same time, the PeRT3's unique architecture utilizes FGPA and signal integrity hardware to communicate with the device under test in the protocol layer. This allows the PeRT3 to perform handshake protocols for loopback initialization, link equalization training and SKP or Align symbol filters for various serial data standards.



De-emphasis and Preshoot

Random Jitter

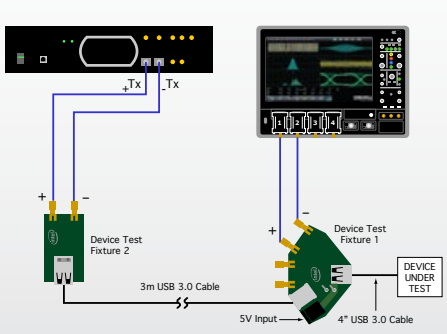
Sinusoidal Jitter

Differential Mode Noise

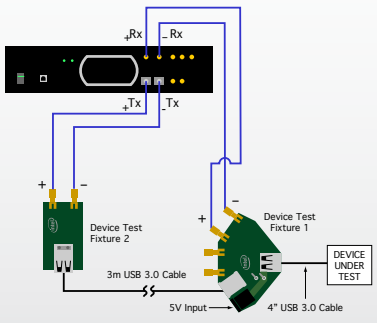
PeRT3 Plays an Important Role in All Areas of Electrical Testing

PeRT3 is the most integrated BER receiver tester with built-in transmitter equalization and jitter sources. At the same time, the protocol awareness capability to handshake with the DUT also allows the PeRT3 to initialize the DUT for transmitter and PLL testing. Most importantly, for serial data standards that require link equalization testing, PeRT3 is the only tool that can combine protocol link training with jitter tolerance and equalization testing.

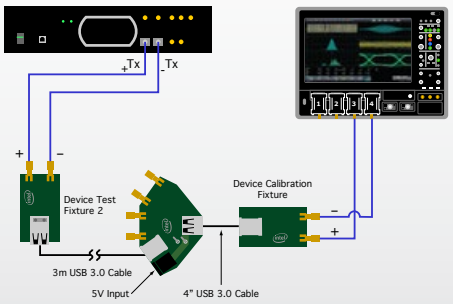
Example of USB 3.0 Transmitter, and Receiver Test and Receiver Calibration Setups



Device Transmitter Compliance Test Setup



Device Receiver Compliance Test Setup



Device Receiver Test Calibration Setup

PeRT³ HARDWARE AND SOFTWARE

1. Generator and Error Detector

PeRT3 generator and receiver provides an extensive list of jitter sources, built-in de-emphasis and pre-shoot for BER testing, and a protocol aware pattern generator and error detector for protocol handshake and link training

2. Clock Output

Full-rate and sub-rate clock can be output for synchronized testing

3. Trigger Output

Trigger output provides programmable trigger states based on BER and the link training state machine

4. Software Control Interface

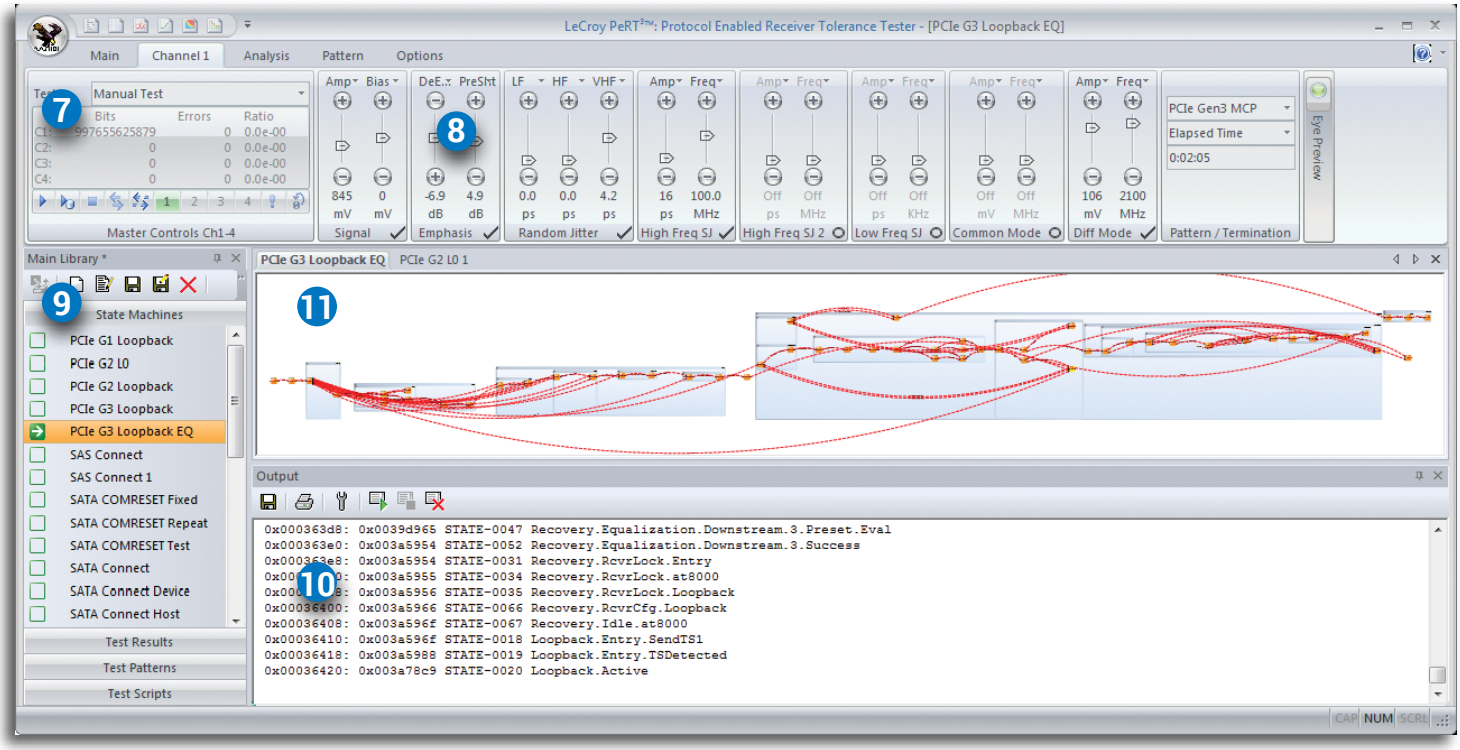
Controlling software can be installed on any PC through a USB interface

5. PCI Express 3.0 Clock Multiplier

PeRT3 has a built-in PCIe Ref Clock input for synchronizing to a PCI Express 3.0 system's master clock for receiver testing

6. Reference Clock

10 MHz Ref clock allows multiple PeRT3 systems to be synchronized for multi-channel testing



7. BER Results Display

Simple BER results display with start, stop, record and error injection controls as well as multiple channel BER display

8. PeRT³ Jitter Sources

All signal controls and jitter sources are displayed in one compact and organized location. All parameters can be adjusted manually in real time or programmed for BER sweep

9. Test Libraries

Test libraries allows the user to create, edit and store test patterns, customized state machines, test scripts and test results

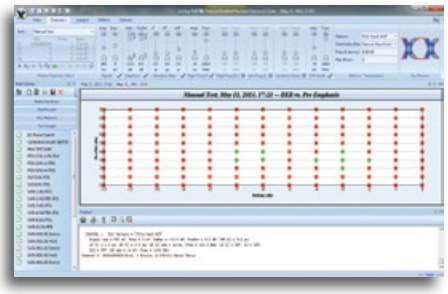
10. Protocol Statement Machine Dialog Output

The dialog box provides the user with a clear status update of the state machine handshake sequence and helps identify where and when the handshake fails

11. Current Test Display

The center of the PeRT3 software can be used to display state machines, test results, test scripts and test patterns

UNIQUE TEST CAPABILITIES

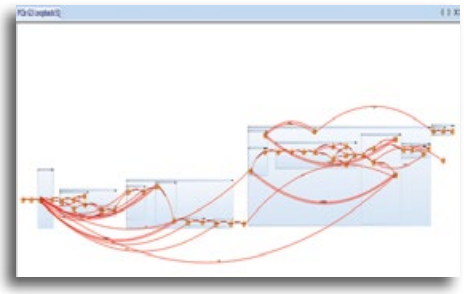


Signal and Jitter Sources

All Signal source and jitter parameters can be swept during BER testing. For example, by sweeping the De-emphasis and Pre-shoot values, the user can identify the optimized equalization window.

Loopback and Link Training Conditions

Each connect sequence provides the user with a list of options to customize the test criteria and debugging conditions.



State View and Editor

Graphical interpretation for the handshake state machine provides fast visual status of handshake status.

Complete Characterization in Development or Automated Test Environments

High-speed serial subsystem design and production is a sophisticated and delicate process of maintaining signal integrity from a transmitter through PCB traces, connectors and cables, and finally to a receiver. The process inevitably introduces deterioration in the signal in the form of increased jitter, electrical noise, reflections from connectors, amplitude fluctuations, timing distortions, and a host of other potential problems.

The design goal for the transmitter is to generate a strong, clean signal that can propagate through the channel and still deliver a quality signal at the other end. The design goal for the receiver is to be able to accurately decode weak signals with the accompanying noise and corruptions that occur in less than optimal connections.

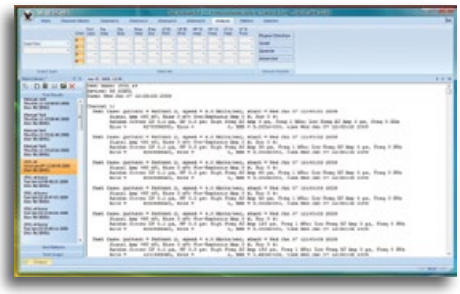
If both goals are accomplished, the result is a reliable and robust communications channel.

There is a set of specifications for each serial data standard (such as PCI Express, SATA, or USB 3.0) that is intended to ensure reliable signal transfer; at the electrical level through eye diagrams and bit error ratio testing, and at the protocol level through error detection schemes such as CRC.

Designers of serial transceivers and users evaluating different designs from different vendors both need a more comprehensive test system that can explore the entire performance envelope of high-speed serial subsystem performance. Confirming that the device alone meets the industry specification is not always sufficient to distinguish between a device that barely passes the specification and a robust system design that has significant margin to allow for real-world variations in conditions and signal quality.

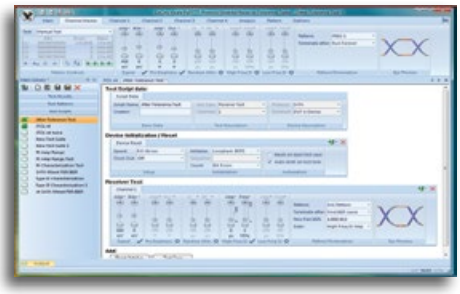
Map the Full Performance Envelope Along Multiple Dimensions

The PeRT3 maps out the full performance envelope of the device under test along multiple dimensions by varying the type and amount of modulation introduced while counting the errors on the returning signal. This provides a GO/NO-GO test and also quantifies the error margins and error susceptibilities of each new design or each tested device. Should failure occur during the test, the environment that caused the failure can be generated by simply highlighting the report, and the design engineer has an environmental setup built to troubleshoot.



Test Log

A full log of the stresses applied to the device under test and the resulting error rates, are all logged against time.



Graphical Test Script Editor

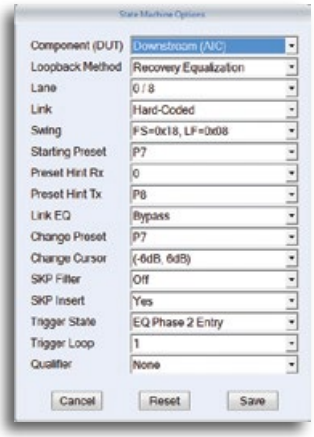
The simple, intuitive interface for creating automated test scripts can, with a few clicks, set up automated tests that initialize the DUT and record error rates while sweeping through any user defined range of jitter parameters.

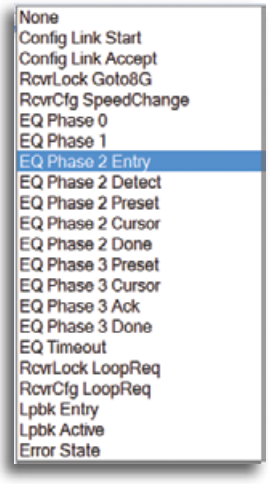
Scatter Chart

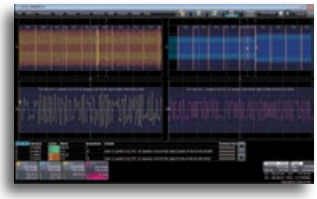
Pass/Fail information is plotted against the stress parameters under test. See what happened for every test case—in real-time.

The Perfect Debugging Tool to Identify a Combination of Protocol and Electrical Issues

PeRT³ programmable State Machine sets up the handshake sequence with DUT → **Setup trigger condition during Link EQ training** → **Trigger the Scope to Capture Upstream and Downstream traffic** → **Decode the Protocol Traffic and crosslink to identify issues between Link Layer and PHY Layer**







In this example, the PeRT³ is programmed to negotiate with the DUT during PCI Express 3.0 link equalization training while all worst case electrical jitter sources are calibrated and turned on. The PeRT³ can then be setup to trigger the oscilloscope based on specific states of the link equalization training. The oscilloscope uses the trigger to capture the upstream and downstream traffic for protocol decode and cross linked protocol and PHY layer analysis.

PCI EXPRESS 3.0 TESTING

New Tools for New Test Requirements

Requirements for serial data testing unique to PCI Express® 3.0 place new demands on the traditional physical layer test tools. Not only does the specification mandate that the receiver tester be protocol aware, but certain other characteristics of PCI Express 3.0, such as dynamic equalization, essentially require combined physical/protocol layer test capabilities for validation and debug. Only Teledyne LeCroy has the comprehensive set of physical layer, protocol layer, and network analysis tools for complete PCI Express 3.0 transmitter, receiver, and channel testing.

Receiver Compliance Testing

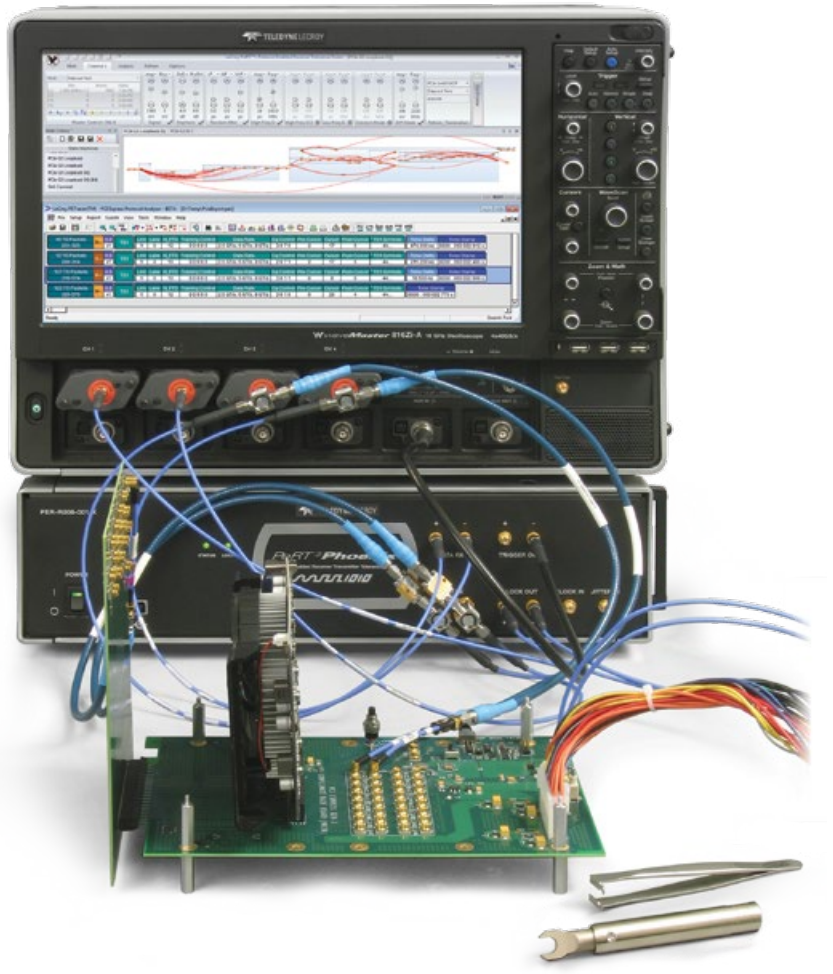
The PeRT3 (Protocol-enabled Receiver and Transmitter Tolerance Tester) fills the space between physical layer test and protocol test, providing a new and more intelligent capability for performance testing of receivers and transmitters.

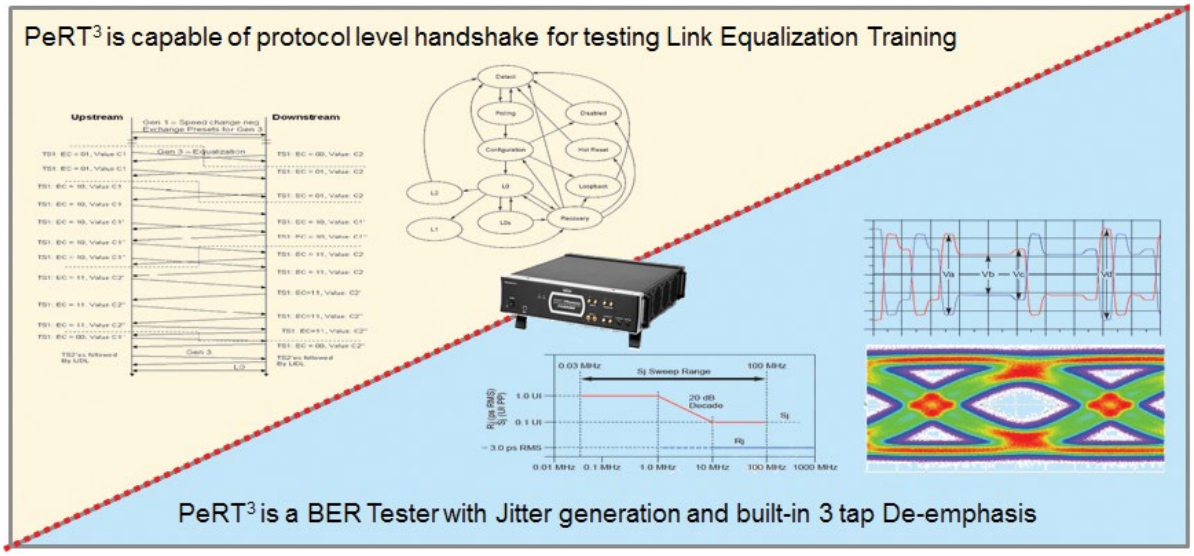
In order to meet the increasingly complex design of today's serial data receivers, the PeRT3 Phoenix expands the bit rate range up to 8.0 Gb/s and offers new signal stress sources and built-in three tap de-emphasis control to address new serial data standards. At the same time, Phoenix continues to focus on protocol awareness to meet the need to communicate with the DUT into proper test modes and train the DUT's receiver equalization setting prior to performing receiver jitter tolerance testing.

Complete Compliance Test Environment

Receiver testing is a critical area for PCI Express 3.0 Compliance. The PeRT3 Phoenix is designed to test the receiver under conditions of proper equalization training, by performing loopback initialization and by introducing different stress types.

Because the system combines protocol awareness with complete stress jitter profile, the PeRT3 Phoenix has revolutionized the receiver testing architecture and has helped to define the PCI Express 3.0 compliance testing methodology.



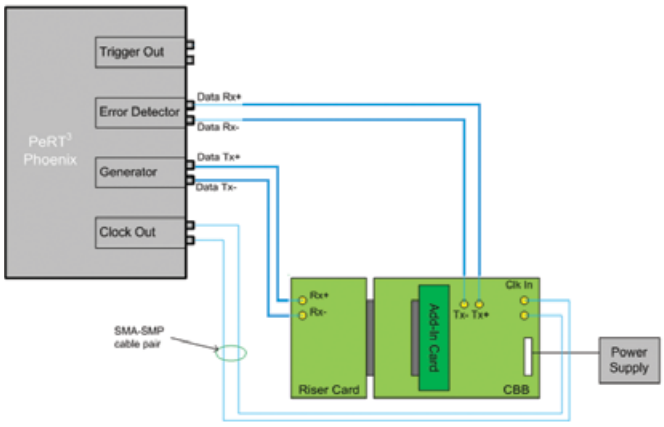


Complete Characterization in Development

The biggest challenge for receiver compliance testing for PCI Express 3.0 is how the receiver performs dynamic equalization training of both the receiver equalization parameters and the proper selection of transmitter equalization presets. The PeRT3 Phoenix can generate both 8b/10b and 128b/130b encoded data to establish PCI Express 3.0 connectivity, and can perform transmitter equalization preset negotiation while the receiver optimizes the receiver equalization parameters. The PeRT3 Phoenix has the unique ability to adjust de-emphasis and preshoot parameters based on preset or cursor requests from the DUT while satisfying the timing requirement per the PCI Express 3.0 specifications, thus making this instrument the perfect tool for validation and characterization of the dynamic equalization design.

Calibrating the Jitter Output of the PeRT3

Receiver test specifications require calibration of the jitter output sources for the test instrument. When using the PeRT3 in conjunction with an SDA 8 Zi-B oscilloscope, this calibration process can be fully automated through the QPHY-PCIe3-TX-RX software option.

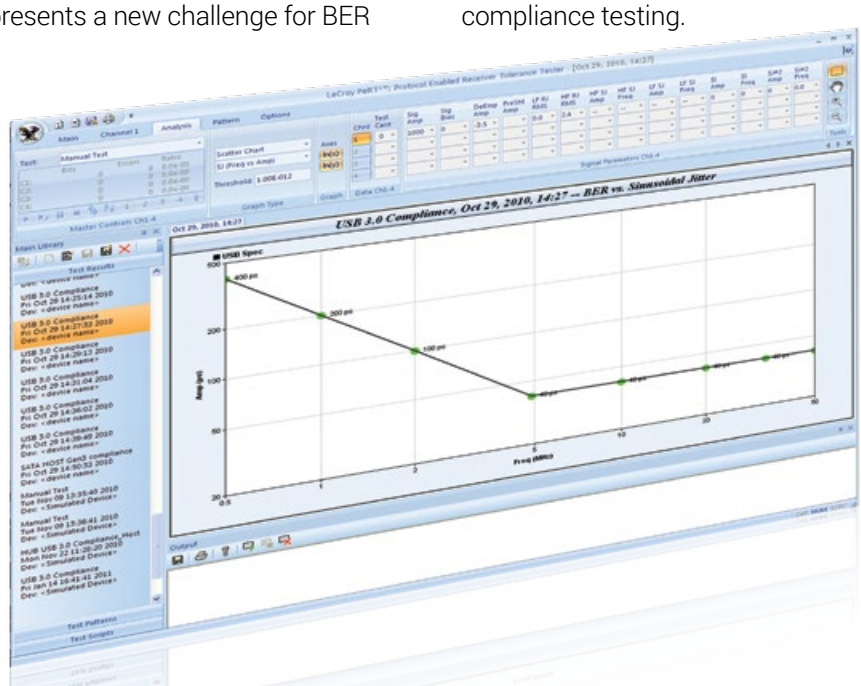


Connection diagram for Receiver Compliance Testing

USB 3.0 TESTING

PeRT³ Value in USB 3.0 Receiver Testing

PeRT³ was the first protocol aware BER test system which enabled SKP or Align filtering during asynchronous receiver test setups. Serial data standards such as USB3.0 and SATA utilize SKP and Align symbols to align recovered and system clocks. This presents a new challenge for BER receiver testers as transmitted and recovered data are different due to SKP or Align Symbols. Combined with an extensive jitter profile and built-in de-emphasis capabilities, the PeRT³ is the most complete and widely adapted solution for USB3.0 Electrical compliance testing.



PeRT³ Value in USB 3.0 Transmitter Testing

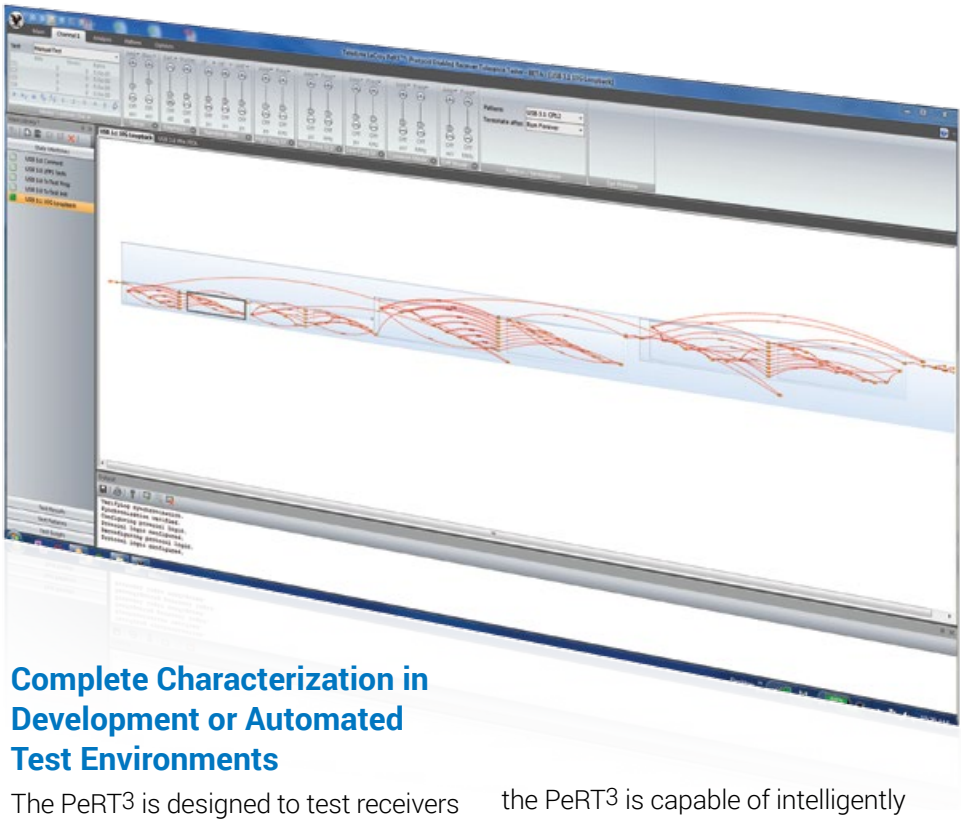
Although, the PeRT³ is primarily used for receiver testing, it can also be used to communicate with the product under test on the protocol layer (Ping. LFPS commands) to stimulate it to output the required compliance patterns for transmitter tests. The transmitter of the PeRT³ can be connected to the receiver of the product under test (PUT), while the transmitter of the product under test is connected to the oscilloscope channels. Using this setup, the SDA 8 Zi-B oscilloscope and the PeRT³ can be combined for automating all of the required transmitter tests.

Calibrating the Jitter Output of the PeRT³

Receiver test specifications require calibration of the jitter output sources for the test instrument. When using the PeRT³ in conjunction with the SDA 8 Zi-B oscilloscope, this calibration is done automatically by the QPHY-USB3-Tx-Rx application.

QualiPHY™

For more information on the USB 3.0 test capabilities of the SDA 813 Zi-B and QPHY-USB3-Tx-Rx, see the document "USB 3.0 Test Solutions QPHY-USB3-Tx-Rx" available from teledynelecroy.com.



Automated State Machine controls DUT and enters USB 3.1 Loopback Mode

First Protocol Aware Receiver Test Solution for SuperSpeed Plus 10Gbps

PeRT3 Phoenix System is the first protocol aware receiver test solution for Superspeed USB 10Gbps (USB 3.1). At 10Gbps, USB3.1 uses a more efficient data encoding scheme and delivers more than twice the effective data rate of USB 3.0, presenting new challenges in receiver testing. The new Teledyne LeCroy PeRT3 Phoenix System simplifies these challenges. PeRT3 Phoenix System supports all the jitter and equalization generation required at 10Gbps, as well as the protocol level handshake that is critical to put the device under test into proper test modes, and under optimal equalization conditions. PeRT3 Phoenix System also offers true SKP symbol injections and SKP filtering during BER testing as well as 128b/132b pattern generation and detection.

Complete Characterization in Development or Automated Test Environments

The PeRT3 is designed to test receivers under conditions of stress by starting with a clean signal and gradually introducing measured levels of a variety of different stress types into the signal, and simultaneously monitoring the bit error rate (BER) to explore the full performance envelope of the receiver system.

Because the system is able to interpret and generate protocol traffic, the PeRT3 is uniquely able to manage fully-automated testing of USB 3.1 products. For example, the PeRT3 can initialize the remote device and command the device to enter or exit loop-back mode while testing is in progress. In addition, the PeRT3 is capable of intelligently managing automated testing through events which disrupt other test systems, such as the addition or deletion of SKP symbols by devices in the data traffic pattern.

With a single integrated system, the PeRT3 replaces up to 6–8 other instruments and greatly simplifies experimental setup, increases the ease of designing and conducting fully automated testing, and provides specific test suites to ensure receiver compliance to USB 3.1 specifications.

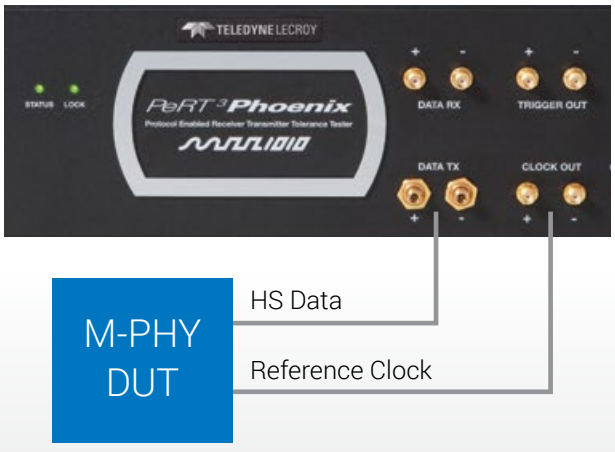
PeRT³ PHOENIX M-PHY RECEIVER TEST SOLUTION

M-PHY Receiver Test

New capabilities of the PeRT3 Phoenix include physical layer receiver testing for the MIPI M-PHY protocol. Added features for M-PHY are support of High Speed GEAR1, GEAR2 and GEAR3, as well as support for Low Speed PWM Mode (G0-G7), auto-calibration and margin testing. Engineers developing next generation mobile devices based on the M-PHY physical layer can now use this solution to resolve design challenges and overcome signal integrity issues by performing automated conformance, product validation and margin tests with ease. Support for HS GEAR1, GEAR2 and GEAR3 and PWM Mode (G0-G7) gives designers the flexibility to perform tests at the full range of data rates for comprehensive insights into their designs. The auto calibration support for high speed GEARs reduces the complexity of setup, saves time, and enables users to test devices faster. Margin testing for high speed gears allows designers to validate and stress their devices to maximum potential resulting in competitive technical specifications for their products.

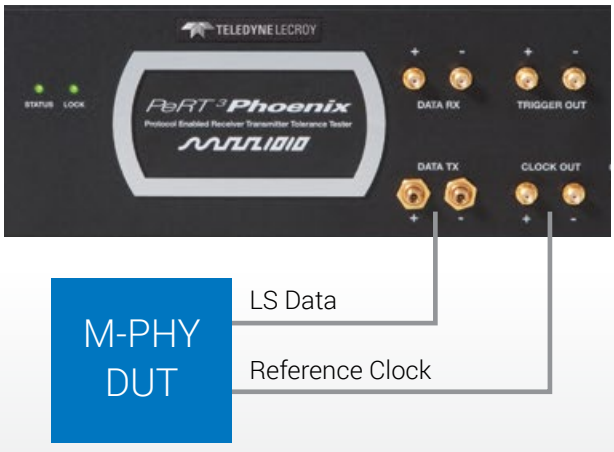
Flexible hardware

Support for M-PHY receiver testing is a simple add on software option to the latest PeRT3 Phoenix hardware platform. The PeRT3 Phoenix Platform is designed to meet the test needs of engineers working with serial data transceivers and other high-speed serial data communication systems. In many new generations of high speed serial I/O standards, the protocol layer controls low power states. The MIPI Alliance's M-PHY specification provides a low-power and low cost PHY solution which is scalable and flexible enough to address existing and future mobile and consumer device markets. With its changeable gears, terminations, amplitudes and high-speed serial data rates, M-PHY presents a number of test challenges on both receiver and transmitter sides that require dedicated test solutions. This requires a PeRT3, a new class of instrumentation that can perform standard receiver tests and also communicate to the transmitter in protocol language. PeRT3 combines all the physical layer capabilities of a BERT system with protocol handshake and training capabilities.



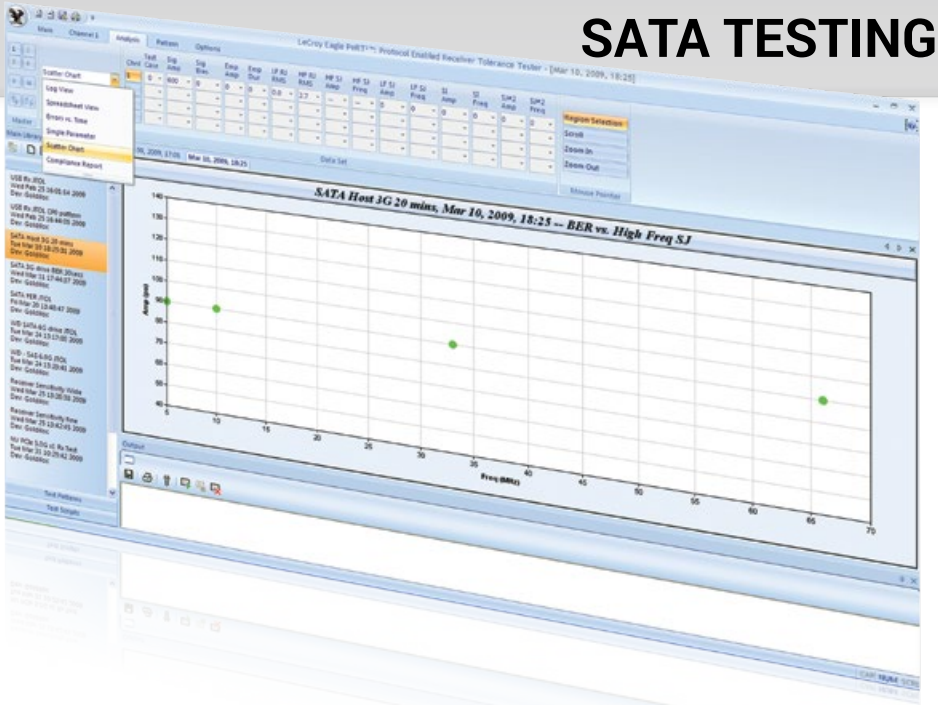
Testing configuration for HS GEAR1/GEAR2/GEAR3

With built-in random jitter sources and deterministic jitter sources, PeRT3 Phoenix delivers a jitter tolerance report to the developer with a click of a button — default setup can be easily customized and saved for future use.



Testing configuration for LS G0-G7

Script-controlled PWM output is the ideal way to verify PWM G0-G7 requirements.



PeRT³ SATA Test System

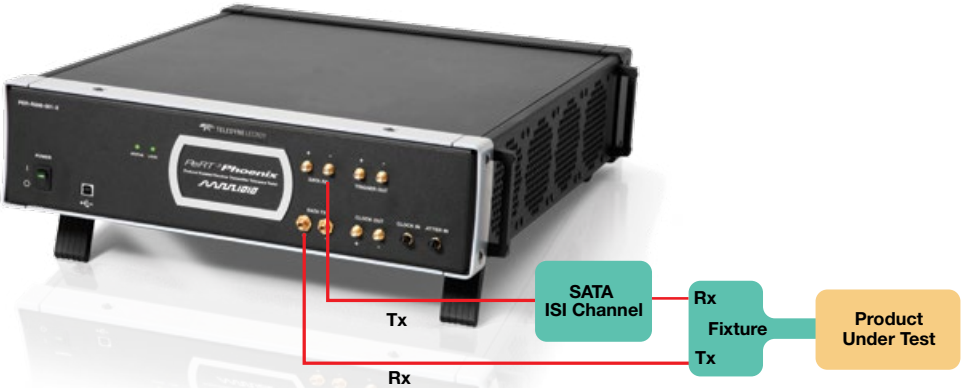
The PeRT³ is designed to test receivers under conditions of stress by starting with a clean signal and gradually introducing measured levels of a variety of different stress types into the signal, and simultaneously monitoring the Frame Error Rate (FER) to explore the full performance envelope of the receiver system.

Because the system is able to interpret and generate protocol traffic, the PeRT³ has the unique capability to manage automated testing of SATA products. For example, the PeRT³ can initialize the PUT and command the PUT to enter or exit loop-back mode while testing is in progress. In addition, the PeRT³ is capable of intelligently managing automated testing through events which may disrupt other test systems, such as the addition or deletion of ALIGN symbols by devices in the data traffic pattern.

Native Frame Error Rate Testing

The PeRT³ allows you to extend testing into protocol areas, such as measuring CRC errors, frame errors and other protocol-specific criteria while actively adding measured amounts of stress into the signal, such as increased jitter and noise. This allows for true native FER testing where the PUT does not need to be in any BIST mode. Instead of loopback, the PeRT³ will send SATA frames to the PUT and wait for the PUT response in terms of CRC, ACK or NACK. Based on these responses, PeRT³ will determine if the frame is successful or not and thereby calculate FER after sending the same Frame repeatedly. There are several advantages in performing true FER testing. First, the test becomes a system level test where both the PHY layer and the protocol layer are tested together as a system. Second, the user can add read or write commands in the Frame and cause the drive to start spinning while testing for jitter tolerance which is a much more stressful and realistic test scenario than any BIST mode compliance tests.

Using a single integrated system, the PeRT³ can replace the Arbitrary Waveform Generator and the FER tester that are typically used for SATA compliance testing. This reduces the investment and makes the test setup much simpler. Furthermore, the PeRT³ can also be used for compliance testing of SAS, USB 3.0, and PCI Express 3.0.



Calibrating the Jitter Output of the PeRT³

Receiver test specifications require calibration of the jitter output sources for the test instrument. When using the PeRT³ in conjunction with the SDA 8 Zi-B oscilloscope, this calibration is done automatically by the QPHY-SATA-TSG-RSG application.

SPECIFICATIONS

PeRT^3 Phoenix

Generator Data Output

Bit Rate	1 Gbps – 10 Gbps Continuous (100 kHz step)
Rise/Fall Time	33 ps typical
Differential Amplitude Range	200 mV to 1.5 V (5 mV step)
Voltage Offset	-2 V to +2 V (5 mV step)
Intrinsic Jitter	1.5 ps RMS RJ (Guaranteed)
Transmitter Equalization	
De-emphasis	0 – 12 dB (0.1 dB step)
Pre-shoot	0 – 9 dB (0.1 dB step)
SSC Support	25 kHz – 35 kHz (500 Hz) (SSC is transferred to the clock output) 500 – 5500 ppm (100 ppm step)
Generator Connector	K-type female
Signal Mode	Differential or single-ended DC coupled, 50 Ω
Error Injection (single bit)	Adds single error on demand

Generator Clock Output

Clock Rate	At rate or divide by 1 – 255
Duty Cycle	40 – 60%
Differential Amplitude Range	0 – 2 Vpp diff (10 mV step)
Voltage Offset	-1 V to 1 V (10 mV step)
Signal Mode	Differential or single-ended DC coupled, 50 Ω
Connector	SMA Female

Generator Jitter Injection

Random Jitter	
LFRJ (Frequency)	10 kHz – 1.5 MHz
LFRJ (Range)	1.5 – 9 ps RMS (0.1 ps step)
HFRJ (Frequency)	1.5 MHz – 100 MHz
HFRJ (Range)	1.5 – 12 ps RMS (0.1 ps step)
PCIERJ (Frequency)	1.5 MHz – 1000 MHz
PCIERJ (Range)	1.5 – 9 ps RMS (0.1 ps step)
Sinusoidal Jitter	
LFSJ (Frequency)	10 kHz – 100 kHz
LFSJ (Range)	100 – 20,000 ps (Jitter is transferred to the clock output)
LFSJ (Frequency)	100 kHz – 1 MHz
LFSJ (Range)	100 – 1500 ps
HFSJ (Frequency)	500 kHz – 180 MHz
HFSJ (Range)	0 – 300 ps (Refer to SJ plots for details)
Common Mode Noise	
CM (Frequency)	100 MHz – 1000 MHz
CM (Range)	50 – 350 mV (5mV step)
Differential Mode Noise	
DM (Frequency)	200 MHz – 2500 MHz
DM (Range)	0 – 140 mV (0.25 dB step)
External Jitter In	
Injected Jitter (Frequency)	0.5 MHz – 100 MHz
Injected Jitter (Range)	1 – 100 ps
Input Impedance	50 Ω
Jitter in Amplitude Limit	600 mV
Signal Mode	DC coupled, 50 Ω
Connector	SMA Female

PeRT^3 Phoenix

Receiver Input

Data Rate	1 Gbps – 10 Gbps
Input Impedance	50 Ω, AC coupled
Amplitude Range Limit	200 – 1800 mV
Repeater	
Data Rate	8G ±5000 ppm
Input Impedance	50Ωs, AC coupled
Amplitude Range Limit	200 – 1800 mV
Equalization	PCI Express 3.0 compliant

Clock and Trigger

Clock-in (At rate)	
Frequency Range	1 GHz – 10 GHz
Input Impedance	50 Ω
Amplitude Range Limit	600-1200 mV
Clock-in (Ref clock)	
Frequency Range	10 MHz ±3 ppm
Input Impedance	50 Ω
Amplitude Range Limit	600-1200 mV
Clock Multiplier (PCIE)	
Frequency Range	100 MHz ± 5000 ppm
PLL Bandwidth	PCIE Gen3 compliant
Input Impedance	50 Ω
Amplitude Range Limit	600 – 1200 mV
Trigger Out / DataTX2	
Single Ended Amplitude	600-800 mV (10 mV step)

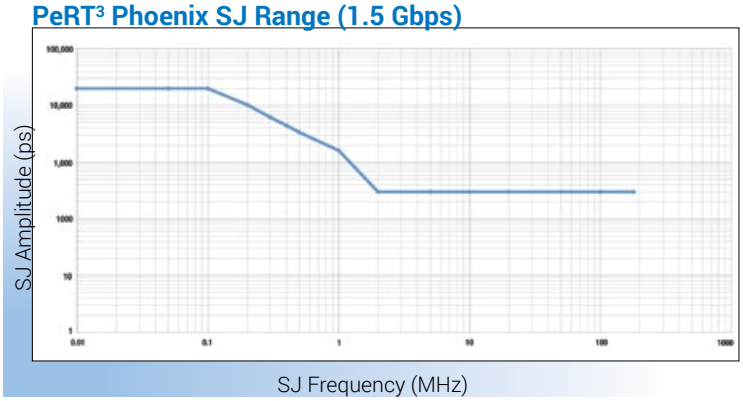
Patterns Contains But Not Limited To The Following

Programmable Custom Pattern Memory	1 Gbyte/Channel
Built in Patterns (Generic)	PRBS5, PRBS7, PRBS9, PRBS11, PRBS15, PRBS20, PRBS23, PRBS31, PRBS5 inverted, PRBS7 inverted, PRBS9 inverted, PRBS11 inverted, PRBS15 inverted, PRBS20 inverted, PRBS23 inverted, PRBS31 inverted, 1 Bit toggle, 2 Bit toggle, 3 Bit toggle, 4 Bit toggle, 5 Bit toggle
Built in Patterns (PCIE)	PCIe G1/G2 Compliance, PCIe Compliance + SKP, PCIe EIEOS, PCIe EIOS, PCIe G2 Logical Idle, PCIe G3 compliance, PCIe G3 Logical Idle, PCIe Gen3 EIEOS, PCIe Gen3 MCP, PCIe Preset Calibration pattern
USB3	USB3.0 CP0, USB3.0 CP1, USB3.0 CP2, USB3.0 CP3, USB3.0 CP4, USB3.0 CP5, USB3.0, CP6, USB3.0 CP7, USB3.0 CP8, USB3.0 BDAT, USB3.0 BRST BDAT BERC, USB3.0 LFPS, USB3.0 LFPS Ping
USB3.1	USB3.1 CP9, USB3.1 CP10, USB3.1 CP11, USB3.1 CP12
M-PHY	CRPAT, CJTPAT
SATA	HFTP, MFTP, LBP, SSOP, Compliance pattern with new LBP, LTDP, LFSCP, JTPAT, Frame loopback pattern
SAS	JTPAT, CJTPAT

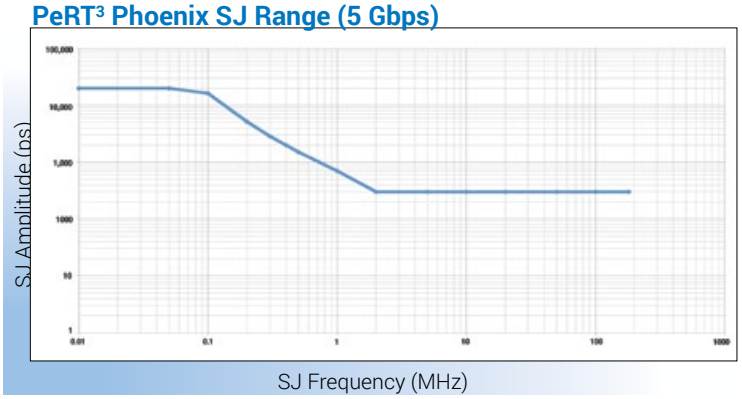
Standard Support

PCI Express 3.0 / 2.0 / 1.0	yes
USB 3.0 Superspeed	yes
USB3.1	10G
SATA Gen1/Gen2/Gen3	yes
SAS 3G/6G	yes

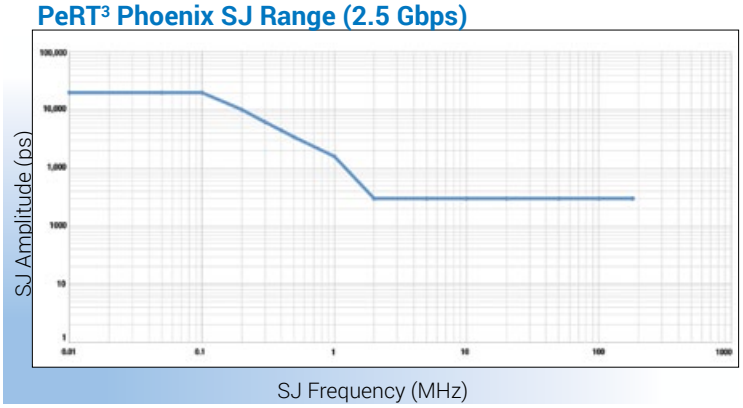
PeRT³ Phoenix SJ Range (1.5 Gbps)



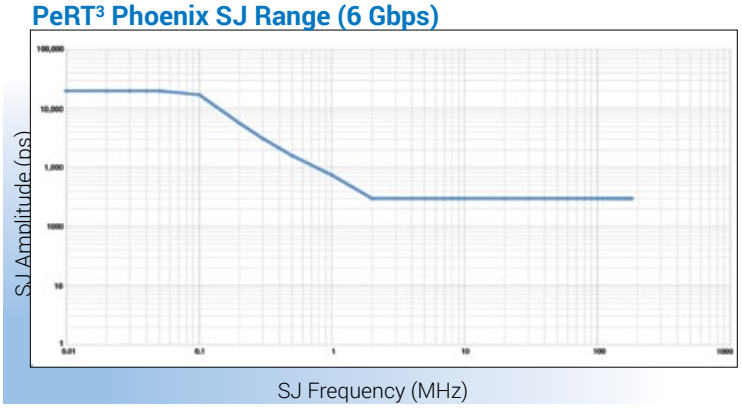
PeRT³ Phoenix SJ Range (5 Gbps)



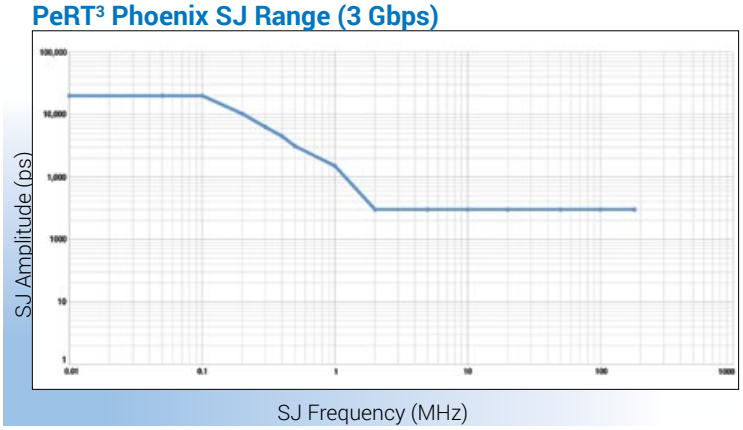
PeRT³ Phoenix SJ Range (2.5 Gbps)



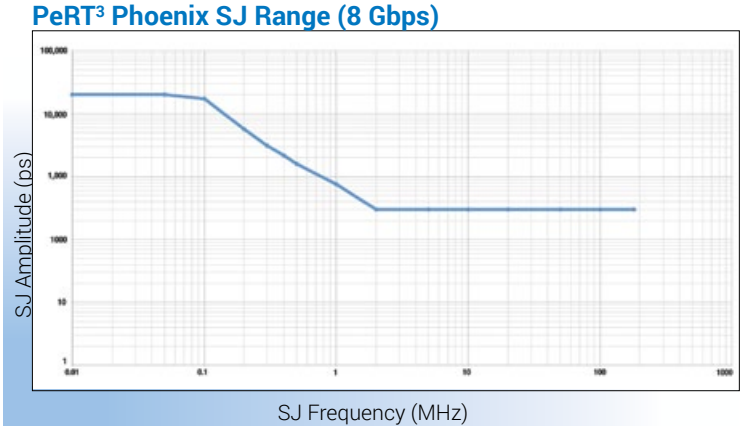
PeRT³ Phoenix SJ Range (6 Gbps)



PeRT³ Phoenix SJ Range (3 Gbps)



PeRT³ Phoenix SJ Range (8 Gbps)



ORDERING INFORMATION

Product Description	Product Code
PeRT³ Phoenix Systems	
PCI Express 1.0/2.0/3.0 System	
Phoenix PeRT 8G System - 1 Channel	PER-R008-S01-X
Receiver Tolerance Test Suite	PER-R006-008-A
PCI Express® 1.0 / 2.0 / 3.0 Receiver Tolerance Test Suite	PCI-R008-004-A
Signal Conditioner for system testing	PER-R008-SCN-X
PCI Express 3.0 Rx Test Accessories	PER-R008-ACS-X
USB 3.X system	
Phoenix PeRT 8G System - 1 Channel	PER-R008-S01-X
Receiver Tolerance Test Suite	PER-R006-008-A
USB 3.0 Receiver Tolerance Test Suite - Phoenix	USB-R008-001-A
Phoenix 10Gbps Option	PER-R008-10G-A
USB 3.1 Test Suite – Phoenix	USB-R008-PLS-A
MIPI M-PHY System	
Phoenix PeRT 8G System - 1 Channel	PER-R008-S01-X
Receiver Tolerance Test Suite	PER-R006-008-A
M-PHY Receiver Test Suite	MPY-R008-S01-A
SATA Gen1/Gen2/Gen3 System	
Phoenix PeRT 8G System - 1 Channel	PER-R008-S01-X
Receiver Tolerance Test Suite	PER-R006-008-A
SATA Receiver Tolerance Test Suite	SAT-R006-004-A
SATA ISI Board	PER-R008-ISI-X
Rise Time Filters	PER-AC06-Q01-X
SAS 3G/6G system	
Phoenix PeRT 8G System - 1 Channel	PER-R008-S01-X
Receiver Tolerance Test Suite	PER-R006-008-A
SAS Receiver Tolerance Test Suite	SAS-R006-004-A
Accessories and Options	
Multi unit synchronization for Phoenix	PER-R008-004-A
SMA to SMA pair Standard Quality	PER-AC12-A01-X
SMA to SMA pair High Quality	PER-AC12-C01-X
SMA to SMP pair	PER-AC12-M01-X
Annual Calibration of PeRT³ Phoenix 8G System	PER-CA08-001-C
Annual Calibration of PeRT³ Phoenix 10G System	PER-CA10-001-C
Three Year Warranty and Two Additional Years Calibration for 1 Channel 8G System	PER-CA08-W01-W
Five Year Warranty and Four Additional Years Calibration for 1 Channel 8G System	PER-CA08-WX1-W
Three Year Warranty and Two Additional Years Calibration for 1 Channel 11G System	PER-CA11-W01-W
Five Year Warranty and Four Additional Years Calibration for 1 Channel 11G System	PER-CA11-WX1-W

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