Tektronix Logic Analyzers

▶ TLA7PG2 Pattern Generator Module

▶ Features & Benefits

64 Channel Modules with Up to 2 Mb Vector Depth

Up to 268 MHz Clock Rate

Supports TTL/CMOS, ECL, PECL/LVPECL, LVDS, LVCMOS Standard Logic Levels

Variable Probe for Supporting Variable Voltage Levels and Delay of Two Channels for Functional Verification

Pattern Sequencing Control of Vector Output Allows Flexible Definition of Complex Events

Works with All TLA700 Series Logic Analyzer Mainframes

▶ Applications

Digital Hardware Verification and Debug

Digital Hardware Simulation and Debug

Breakthrough Solutions for Real-time Digital Systems Analysis

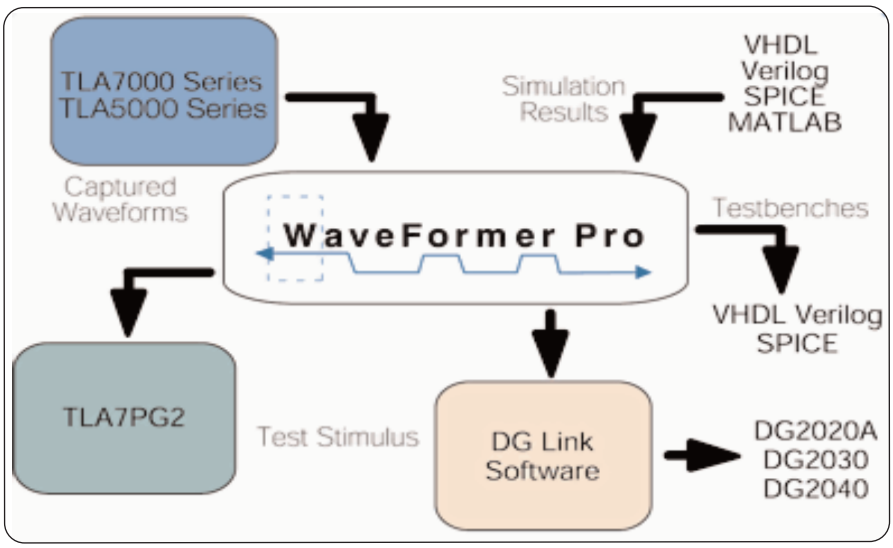
Hardware and software engineers need the ability to generate digital stimuli to simulate infrequently encountered test conditions in hardware design and software program testing. A pattern generator enables you to perform functional verification, debugging and stress testing for system hardware design. This multi-channel, programmable pattern generator module with sequential control stimulates a prototype with data from a simulator for extended analysis. The pattern generator is ideal for designing systems where surrounding boards, ICs or buses that normally provide digital signals to the device under test are missing. With the pattern generator, you can place a circuit in a desired state, operate it at full speed or single-step it through a series of states.

The TLA7PG2 features 64 channels and supports up to a 268 MHz clock rate for data output. The TLA7PG2 is made compatible with numerous voltage levels and technologies through the use of external pattern generator probes.

The TLA7000 Series logic analyzers capture waveform data in a form that can be read by SynaptiCAD WaveFormer Pro, VeriLogger Pro and TestBencher Pro software tools. SynaptiCAD's tools can convert the logic analyzer waveform data into stimulus vectors for VHDL, Verilog, SPICE, ABEL and pattern generators, including the TLA7PG2. This functionality gives engineers the ability to leverage the work done during the design phase of a product, simplifying the development of a hardware test environment that provides complete test coverage and excellent debug capability.

Tektronix

Enabling Innovation



▶ Easily Create TLA7PG2 Stimulus Files – The TLA7PG2 Pattern Generator stimulus can be created from a mixture of VHDL and Verilog test benches, simulation waveforms, real world data acquired by a logic analyzer and waveforms created within SynaptiCAD's timing diagram editing environment.

▸ Characteristics

General

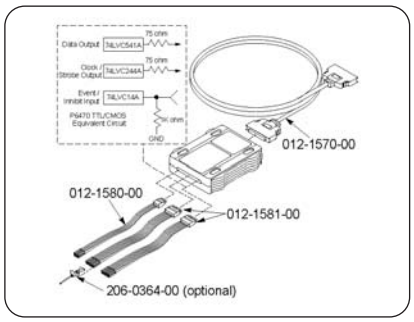
Data Width –
64 Channel full channel mode.
32 Channel half channel mode.
Module "Merging" – Up to five modules can be "merged" to make up to a 320 channel module. Merged modules exhibit the same depth as the lesser of the 5 individual modules.
Number of Mainframe Slots Required – 2.
Data Rate – Internal Clock:
0.5 Hz to 134 MHz full channel mode.
1.0 Hz to 268 MHz half channel mode.
External Clock:
DC to 134 MHz full channel mode.
DC to 268 MHz half channel mode.
External Clock Input –
Polarity: positive or negative.
Threshold: –2.56 V to +2.54 V, nominal; programmable in 20 mV increments.
Sensitivity: <500 mV_{p-p}.
Impedance: 1 kΩ terminated to ground.
Data Depth –
256 Kb full channel/512 Kb half channel.
1 Mb full channel/2 Mb half channel (optional).

Pattern Sequencing Characteristics

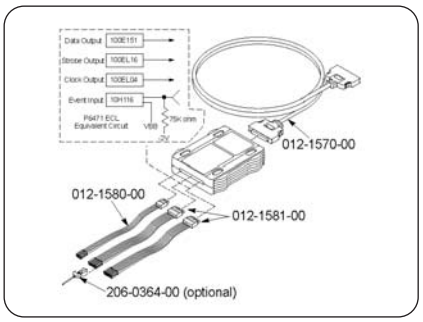
Blocks – Separate sections of pattern program that are output in a user definable order by the Sequencer. Block pattern depth can be from 40 sequences (full channel mode) or 80 sequences (half channel mode) up to the entire depth of the TLA7PG2. A maximum of 4,000 Blocks may be defined.
Sequencer – A 4,000 line memory that allows the user to pick the output order of individual Blocks. Each line in the sequencer allows the definition of a Block to be output, a Repeat Count for that Block, A Wait For event condition for the Block, the Signal state for that Block (asserted or unasserted), and a Jump If event Condition, with a sequence line to jump to if the condition is satisfied.
Sub-sequences – Up to 256 contiguous lines of the Sequencer memory may be defined as a Sub-sequence. A Sub-sequence can then be treated like a block. (Example: 15 Sequences of Blocks are defined as Sub-sequence A1. Now any line in the Sequencer can output A1. Five calls to Sub-sequence A1 will be flattened out to 75 sequences at run time.)
Jump If – Jumps to the specified sequence if a user defined event is true. The user defined event is a boolean combination of the eight external event input.
Wait For – Pattern output is paused until the user defined Event is true. One Wait For may be defined for every Block.
Assert Signal – One of the four inter-module signals is selected to be controlled from the pattern generator program. Signals may be asserted and unasserted allowing true interaction with the logic analyzer modules and with other pattern generator modules. Signal action (assert or unassert) may be defined for every Block.
Repeat Count – The sequence is repeated from 1 to 65,536 times. Infinite may also be selected. One Repeat Count may be defined for every block. Note that a repeat value of 10,000 takes one sequence line in memory, not 10,000.
Step – While in Step mode, the TLA7PG2, the user can manually satisfy (i.e., click an icon) Wait For and Jump conditional events. This allows the user to debug the logic flow of the program's sequencing.
Initialization Block – The unconditional Jump command allows the user to implement an equivalent function.
Logic Analyzer/Pattern Generator Connectivity to Simulation Environments – The TLA600 and TLA700 Series logic analyzers capture waveform data in a form that can be read by SynaptiCAD WaveFormer Pro, VeriLogger Pro, and TestBencher Pro software tools. SynaptiCAD's tools can convert the logic analyzer waveform data into stimulus vectors for VHDL, Verilog, SPICE, ABEL, and pattern generators including the TLA7PG2.
SynaptiCAD's WaveFormer Pro product offers a timing diagram editing environment that enables stimulus to be created using a combination of graphically drawn signals, timing parameters that constrain edges, clock signals and temporal and Boolean equations for describing complex, quasi-repetitive signal behavior. Advanced operations on signals such as time scaling and shifting, and block copy and pasting of signal behavior over an interval of time are also supported.

P6470 TTL/CMOS Probe

Number of Data Outputs –
16 in Full Channel Mode.
8 in Half Channel Mode.
Number of Clock Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Number of Strobe Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Clock Output Polarity – Positive.
Strobe Type – RZ only.
Strobe Delay – Zero or Trailing Edge.
Output Type –
HD74LVC541A for Data Output.
HD74LVC244A for Clock/Strobe Output.
Rise/Fall Time (20% to 80%) – Timing values measured using 75 Ω termination (internal to probe), 1 MΩ + <1 pF load and VOH set to 5.0 V
Clock/Strobe Output –
Rise: 640 ps typical.
Fall: 1.1 ns typical.
Data Output –
Rise: 680 ps typical.
Fall: 2.9 ns typical.
Rise/Fall Time (20% to 80%) – Timing values measured using 75 Ω termination (internal to probe), 510 Ω + 51 pF load and V_{OH} set to 5.0 V.
Clock/Strobe Output –
Rise: 6.5 ns typical.
Fall: 6.3 ns typical.
Data Output –
Rise: 5.2 ns typical.
Fall: 4.5 ns typical.
Series Terminator Resistor – 75 Ω standard; 43, 100 and 150 Ω optional.
Output Voltage (nominal, load: 1 MΩ) – V_{OH}. 2.0 V to 5.5 V, tri-statable, programmable in 25 mV increments.
Data Output Skew –
<570 ps typical between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<440 ps typical between all data output pins of single probe.
Data Output to Strobe Output Delay – 1.7 ns typical when strobe delay set to zero.
Data Output to Clock Output Delay – 2.4 ns typical.
External Clock Input to Clock Output Delay –
Full channel mode: 61 ns typical.
Half channel mode: 61 ns typical.
Number of External Event Inputs – 1.
Number of External Inhibit Inputs – 1.



▶ P6470.



▶ P6471.

External Inhibit Input to Output Enable Delay – 34 ns typical for Data Output.
External Inhibit Input to Output Disable Delay – 86 ns typical for Data Output.
Probe D Data Output to Output Enable Delay – (for Internal Inhibit) 7 ns typical for Data Output.
Probe D Data Output to Output Disable Delay – (for Internal Inhibit) 8 ns typical for Data Output.
External Event Input to Clock Output Setup (for inhibit) (event-filter: off) –
Full channel mode: 1.5 clocks + 240 ns typical.
Half channel mode: 2 clocks + 240 ns typical.
External Event Input and Inhibit Input –
Input Type: 74LVC14A.
Minimum Pulse Width: 200 ns.

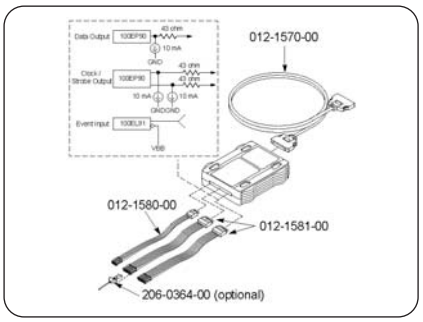
P6471 ECL Probe

Number of Data Outputs –
16 in Full Channel Mode.
8 in Half Channel Mode.
Number of Clock Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Number of Strobe Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Clock Output Polarity – Positive.
Strobe Type – RZ only.
Strobe Delay – Zero or Trailing Edge.
Output Type –
100E151 for data output.
100EL16 for strobe output.
100EL04 for clock output.
All outputs are unterminated.
Rise/Fall Time (20% to 80%) – Timing values measured using 51 Ω to –2.0 V.
Clock Output –
Rise: 320 ps typical.
Fall: 330 ps typical.
Data Output –
Rise: 1200 ps typical.
Fall: 710 ps typical.
Strobe Output –
Rise: 290 ps typical.
Fall: 270 ps typical.
Data Output Skew –
<255 ps typical between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<210 ps typical between all data output pins of single probe.
Data Output to Strobe Output Delay – 2.94 ns typical when strobe delay set to zero.
Data Output to Clock Output Delay – 780 ps typical.
External Clock Input to Clock Output Delay – 50 ns typical.
Number of External Event Inputs – 2.
External Event Input –
Input Level: ECL. Terminated with 75 KΩ, –2V.
Input Type: 10H116.
Minimum Pulse Width: 150 ns.

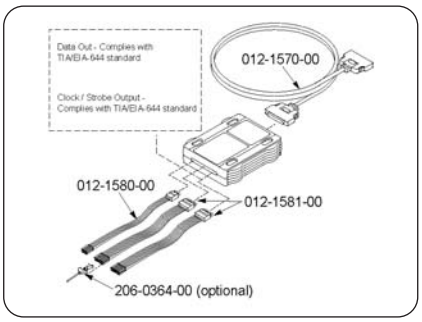
P6472 PECL/LVPECL Probe

Number of Data Outputs – 8 in full channel mode or half channel mode.
Number of Clock Outputs – 1. (Only one of clock output and strobe output can be enabled.)
Number of Strobe Outputs – 1. (Only one of clock output and strobe output can be enabled.)
Number of External Event Inputs – 2.
Number of External Inhibit Inputs – 0.
Clock Output Polarity – Positive.
Strobe Type – RZ only.
Strobe Delay – Zero or Trailing Edge.
Output Type –
100EP90 for data output.

100EP90 for clock/strobe output.
Rise/Fall Time (20% to 80%) –
Rise: 330 ps typical.
Fall: 970 ps typical.
Output Voltage Level – PECL, LVPECL.
Data Output Skew –
<385 ps between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<370 ps between all data output pins of all probes of a single module.
<340 ps between all data output pins of a single probe.
Data Output to Strobe Output Delay – +2.93 ns when strobe delay set to zero.
Data Output to Clock Output Delay – +1.12 ns.
External Clock Input to Clock Output Delay – 50 ns.
Event Input Voltage Level – PECL, LVPECL.
Input Type – 100EL91, unterminated.
Minimum Pulse Width – 150 ns.



► P6472.



► P6473.

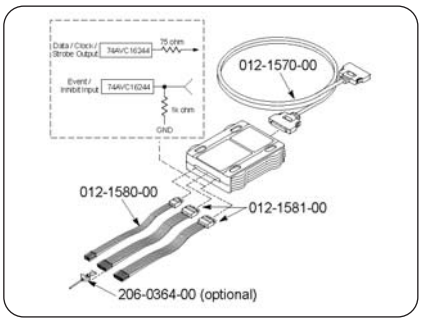
P6473 LVDS Probe

Number of Data Outputs –
16 in Full Channel Mode.
8 in Half Channel Mode.
Number of Clock Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Number of Strobe Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Clock Output Polarity – Positive.
Strobe Type – RZ only.
Strobe Delay – Zero or Trailing Edge.
Number of External Event Inputs – 1.
Number of External Inhibit Inputs – 1.
Output Type –
LVDS (TIA/EIA-644 compatible) for data output.
LVDS (TIA/EIA-644 compatible) for clock/strobe output.
Rise/Fall Time (20% to 80%) –
Rise: 910 ps typical.
Fall: 750 ps typical.
Data Output Skew –
<365 ps between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<350 ps between all data output pins of all probes of a single module.
<320 ps between all data output pins of a single probe.
Data Output to Strobe Output Delay – –280 ps when strobe delay set to zero.
Data Output to Clock Output Delay – 1.2 ns.
External Clock Input to Clock Output Delay – 55 ns.
External Inhibit to Output Enable Delay – 9 ns for data output.
External Inhibit Input to Output Disable Delay – 12 ns for data output.
Probe D Data Output to Output Enable Delay – 2 ns for data output.
Probe D Data Output to Output Disable Delay – 5 ns for data output.
External Event Input to Clock Output Setup –
Full Channel Mode: 1.5 Clocks + 180 ns.
Half Channel Mode: 2 Clocks + 180 ns.
External Event Input and Inhibit Input –
Input Type: LVDS, positive true.
Minimum Pulse Width: 150 ns.

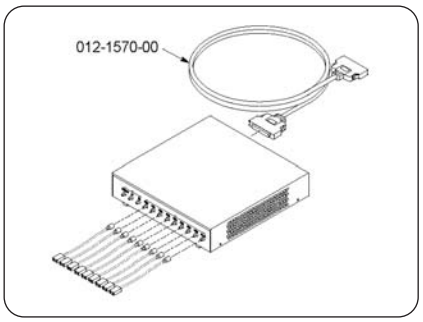
P6474 LVCMOS Probe

Number of Data Outputs –
16 in Full Channel Mode.
8 in Half Channel Mode.
Number of Clock Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Number of Strobe Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)
Clock Output Polarity – Positive.
Strobe Type – RZ only.
Strobe Delay – Zero or Trailing Edge.
Number of External Event Inputs – 2.
Number of External Inhibit Inputs – 1.
Output Type – 74AVC16244 for data, clock, strobe outputs.
Series Terminator Resistor – 75 Ω standard. 43, 100, and 150 Ω optional.

Rise/Fall Time (20% to 80%) –
Load: 1 MΩ + <1 pF
Rise: 1.2 ns
Fall: 610 ps typical
Load: 510 Ω + 20 pF
Rise: 3.4 ns
Fall: 3.2 ns
Output Voltage Level –
1.2 V to 3.3 V, 25 mV step, into 1 MΩ.
Data Output Skew –
<590 ps between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<500 ps between all data output pins of all probes of a single module.
<460 ps between all data output pins of a single probe.
Data Output to Strobe Output Delay – 460 ps when strobe delay set to zero.
Data Output to Clock Output Delay – 1.84 ns.
External Clock Input to Clock Output Delay – 55 ns.
External Inhibit to Output Enable Delay – 36 ns for data output.
External Inhibit Input to Output Disable Delay – 18 ns for data output.
Probe D Data Output to Output Enable Delay – 6 ns for data output.
Probe D Data Output to Output Disable Delay – 7 ns for data output.
External Event Input to Clock Output Setup –
Full Channel Mode: 1.5 clocks + 180 ns.
Half Channel Mode: 2 clocks + 180 ns.
External Event Input and Inhibit Input –
74AVC16244, Positive True, 1 kΩ to ground.
The V_{cc} of the input receiver is variable and is the same as the output driver.
Minimum Pulse Width: 150 ns.



▶ P6474.



▶ P6475.

P6475 Variable Probe

Rise/Fall Time (20% to 80%) –
Load: 1 MΩ + <1 pF
Rise: 550 ps
Fall: 640 ps
Load: 50 Ω
Rise: 430 ps
Fall: 510 ps
Output Voltage Level –
V_{OL}: –3 V to 6.5 V, 10 mV step, into 1 MΩ.
V_{OH}: –2.5 V to +7 V, 10 mV step, into 1 MΩ.
Output Voltage Swing – 250 mV_{p-p} to 9 V_{p-p}.
Output Voltage Control –
Ch. 0 to Ch. 5: Common.
Ch. 6 to Ch. 7, clock: Independent.
Accuracy – ±3% of value ±0.1 V.
Delay Channels – Ch. 6 and Ch. 7 (Independent).
Delay Time – 0 ns to 50 ns with reference to Ch. 0.
Ch. 6 Output Modes – Normal.
Ch. 6 OR Ch. 7.
Ch. 6 AND Ch. 7.
Ch. 6 OR (NOT Ch. 7).
Ch. 6 AND (NOT Ch. 7).
Delay Accuracy – ±(3% of Delay Time) ±0.8 ns (to Ch. 0). (At maximum slew rate setting.)
Slew Rate Control – 0.5 V/ns to 2.5 V/ns, 100 mV/ns step.
Data Output Skew –
<295 ps between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<280 ps between all data output pins of all probes of a single module.
<250 ps between all data output pins of a single probe.
Data Output to Clock Output Delay – 940 ps.
External Clock Input to Clock Output Delay – 62 ns.
Number of External Event Inputs – 2.
Number of External Inhibit Inputs – 1.
External Inhibit to Output Enable Delay – 30 ns for data output.
External Inhibit Input to Output Disable Delay – 28 ns for data output.
Probe D Data Output to Output Enable Delay – –100 ps for data output.
Probe D Data Output to Output Disable Delay – –4.4 ns for data output.
External Event Input to Clock Output Setup –
Full Channel Mode: 1.5 Clocks + 180 ns.
Half Channel Mode: 2 Clocks + 180 ns.
External Event Input and Inhibit Input –
Polarity: Positive True.
Impedance: 1 kΩ to ground.
Threshold Level: –2.5 V to +2.5 V, Event and Inhibit are independent.
Threshold Resolution: 20 mV.
Minimum Pulse Width: 150 ns.
Safety –
CSA C22.2 No. 1010.1, EN61010-1, IEC61010-1, UL 3111-1.

Physical Characteristics for TLA7PG2

Dimensions	**mm**	**in.**
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3	6.5
Shipping	6.2	13.5

P6470 Probe Cable Length – 1.6 m (5 ft.).
P6471 Probe Cable Length – 1.6 m (5 ft.).
P6472 Probe Cable Length – 1.6 m (5 ft.).
P6473 Probe Cable Length – 1.6 m (5 ft.).
P6474 Probe Cable Length – 1.6 m (5 ft.).
P6475 Probe Cable Length – 1.6 m (5 ft.).

▸ Ordering Information

TLA7PG2

64-Channel pattern generator module, 134 MHz data rate, 256 Kb depth (please select probe option below).

Includes: Four probe cables, certificate of calibration, one year warranty (return to Tektronix), and user manual.

Options

Opt. 1M – Increase to 1 Mb depth.

Probes are sold separately.

Other Accessories

TLA7PG2 Pattern Generator Module Performance Verification and Adjustment Fixture – Order 067-A018-00.

TLA7PG2 Pattern Generator Module Service Manual (includes performance verification and adjustment procedures) – Order 071-0714-01.

TLA Series Pattern Generator Module(s) Upgrades

You can increase the memory depth of most existing TLA7000 Series pattern generator modules. You can also install a TLA7PG2 pattern generator module into an existing TLA715/721/7XM/7012/7016 mainframe. Please refer to the TLA Family Upgrade Guide for further details.

TLA7PG2 Service Options

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

TLA7PG2 Pattern Generator Probes

Probes are sold separately.

16-Channel TTL/CMOS Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6470. Refer to diagram on Page 3.
- 8-Channel leadsets (2 each) – Order 012-1581-00.
- 5-Channel leadset (1 each) – Order 012-1580-00.
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Pattern Generator Probe User Manual – Order 071-1017-01.

16-Channel ECL Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6471. Refer to diagram on Page 3.
- 8-Channel leadsets (2 each) – Order 012-1581-00.
- 5-Channel leadset (1 each) – Order 012-1580-00.
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Pattern Generator Probe User Manual – Order 071-1017-01.

8-Channel PECL/LVPECL Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6472. Refer to diagram on Page 4.
- 8-Channel leadset (1 each) – Order 012-1581-00.
- 5-Channel leadset (1 each) – Order 012-1580-00.
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Pattern Generator Probe User Manual – Order 071-1017-01.

16-Channel LVDS Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6473. Refer to diagram on Page 4.
- 8-Channel leadsets (2 each) – Order 012-1581-00.
- 5-Channel leadset (1 each) – Order 012-1580-00.
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Pattern Generator Probe User Manual – Order 071-1017-01.

16-Channel LVCMOS Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6474. Refer to diagram on Page 5.
- 8-Channel leadsets (2 each) – Order 012-1581-00.
- 5-Channel leadset (1 each) – Order 012-1580-00.
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Pattern Generator Probe User Manual – Order 071-1017-01.

8-Channel Variable Probe and Accessories for TLA7PG2 Pattern Generator Module – Order P6475. Refer to diagram on Page 5.
- SMB-to-header coaxial cable set. Order 012-1504-00
- Probe Cable – Optional. Standard with TLA7PG2 module. Order 012-1570-00.
- Time Alignment Cable for use with P6470/P6473/P6474. Order 012-A224-00.

Tektronix Logic Analyzers

► TLA7PG2 Pattern Generator Module

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www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

05/05 DV/WOW 52W-15056-5

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