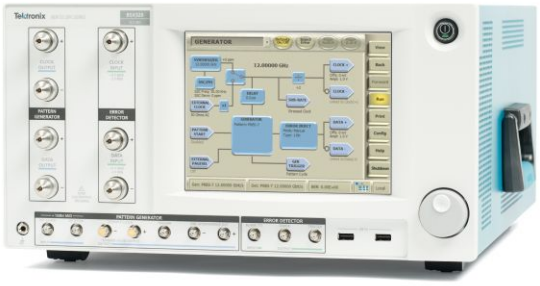
Tektronix®

Bit Error Rate Tester

BSX Series BERTScope® Datasheet



The BERTScope BSX-series Bit Error Rate Tester introduces a receiver test platform capable of supporting emerging Gen4 standards and beyond. With the addition of powerful data processing and internal Tx equalization, the BERTScope supports protocol-based handshaking and synchronization with your device under test (DUT), including interactive link training at data rates up to 32 Gb/s. The BSX-series shortens the time to debug physical layer and link training issues, and provides the quickest path to compliance for a broad range of standards.

Notice to EU customers

This product is not updated to comply with the RoHS 2 Directive 2011/65/EU and will not be shipped to the EU. Customers may be able to purchase products from inventory that were placed on the EU market prior to July 22, 2017 until supplies are depleted. Tektronix is committed to helping you with your solution needs. Please contact your local sales representative for further assistance or to determine if alternative product(s) are available. Tektronix will continue service to the end of worldwide support life.

Key performance specifications

- Pattern Generation and Error Analysis up to 32 Gb/s
- Optional built-in 4-tap Tx equalization with support for interactive link training
- Protocol-oriented and bit-oriented multi-chain pattern sequencing with enhanced pattern/sequence editor
- User-defined detector pattern matching with stimulus-response feedback
- Patented Error Location Analysis™ goes beyond BER measurement to provide insight into the sources of errors through analysis of correlations and deterministic error patterns
- Optional Forward Error Correction analysis provides for simulation of post-FEC error rate based upon measured error location patterns
- Integrated Eye Diagram Analysis with BER Correlation including Mask Testing, Jitter Peak, BER Contour
- Optional Jitter Map Comprehensive Jitter Decomposition - with Long Pattern (i.e. PRBS-31) Jitter

Key features

- Provides a single solution for Receiver stress testing, debug and compliance
- Test Gen3 and Gen4 standards including PCIe, SAS, and USB3.1 and proprietary standards
- DUT handshaking capability above16 Gb/s supporting RX test requirements for loopback initiation and adaptive link training for key standards such as PCIe
- Protocol-aware pattern generation and error detection supports flexible stimulus response programmability and debugging of handshaking issues.
- Forward error correction (FEC) emulation option supports measurement of BER both before and after error correction for commonly used Reed-Solomon FEC codes.
- Calibration and test automation software available for key standards

Applications

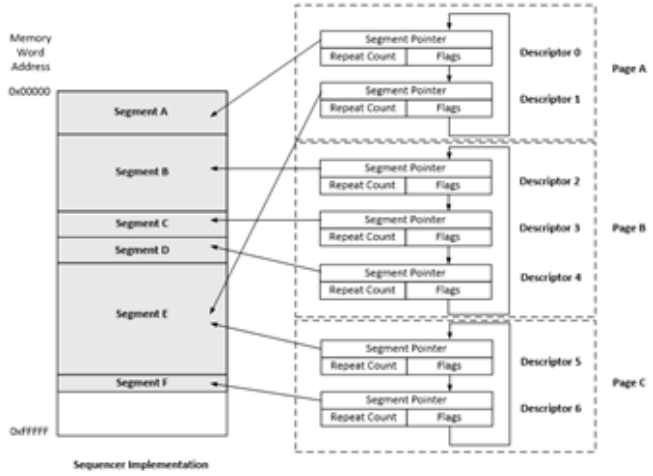
- Design verification including signal integrity, jitter, and timing analysis
- Design characterization for high-speed, sophisticated designs
- Design/Verification of high-speed I/O components and systems including DUT handshaking
- Signal integrity analysis – mask testing, jitter peak, BER contour, jitter map, and forward error correction emulation

Intelligent memory sequencing

With both Bit Oriented and Protocol Aware memory sequencing modes available, and the ability to advance the sequencer based on a user-defined detector pattern match, the BSX series allows the user to create their own protocol-based patterns and handshaking sequences.

Pattern memory sequencer

The BSX-series memory sequencer implements flexible indirect access to pattern memory. The pattern memory can support two levels of loop nesting with up to 1 million iterations per loop. To further simplify programming and increase memory efficiency, individual pattern segments can be any size greater than 128 bits. Advancement of the memory sequence can be controlled by software control, external signal, or detector pattern match providing the user with multiple means for controlling handshaking with test devices.



Memory sequencer modes

To provide the user with more flexibility and simplicity in creating and detecting patterns and sequences, two distinct sequencer modes are offered, with both supporting the looping and sequence advance features described above:

- Bit Oriented Sequencer mode. In bit-oriented mode, bits are sent unaltered from pattern memory to the Generator output with no protocol processing applied. This is equivalent to traditional BERT memory pattern operation.
- Protocol Aware Sequencer mode. In protocol-aware mode, pattern memory words are treated as protocol blocks or groups of symbols, instead of bits. Words are fetched from memory and processed according to the selected protocol or encoding. Depending upon the specific protocol requirements, protocol-oriented mode processing may include:
  - Packaging of symbols into protocol blocks
  - Symbol encoding
  - Data scrambling
  - DC balancing

  This allows the user to input memory data in a “natural” format. Note that transition between sequencer states can be made without regard to data “stitching” problems since the sequencer maintains scrambling/DC balancing states.

Detector pattern matching

The BSX-series supports optional user-defined Detector pattern matching which can be used to advance the Generator sequencer state. This capability allows flexible stimulus/response programmability to support debugging and proprietary protocols. As with the memory sequencer, the pattern matching supports two modes:

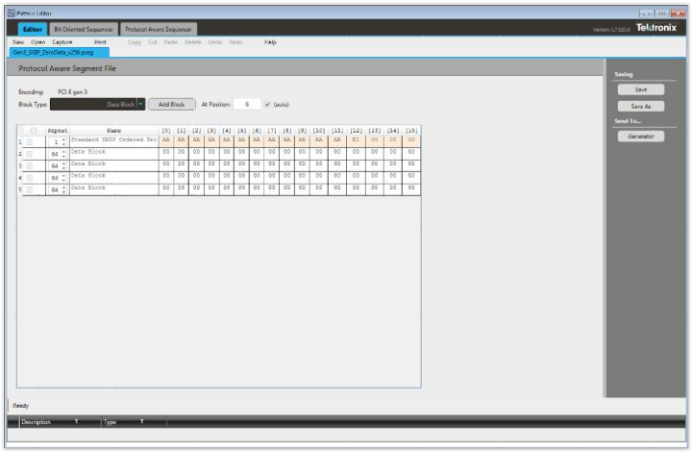
- Bit Oriented matching mode. Bit-oriented mode includes four general-purpose Detector pattern matchers capable of finding any arbitrary pattern up to 128 bits in length in the incoming data stream, with bit masking available. A match can cause the sequencer to advance to the next state.
- Protocol Aware matching mode. Protocol-aware mode includes sixteen Detector pattern match elements for protocol-based pattern matching. For PCIe Gen3/4 and USB 3.1 Gen2, the Detector can match the entire decoded block payload, with bit/byte masking. For 8b/10b encoding, the detector can match up to 16, 8-bit symbols after block/symbol decoding with masking.

Protocol block/symbol filtering

Supported protocols have clock compensation (skip) and block/symbol filtering implanted, as is often required for independent clock operation. A protocol-filtering toggle in the Detector switches between raw bitstream and filtered bitstream for BER measurement.

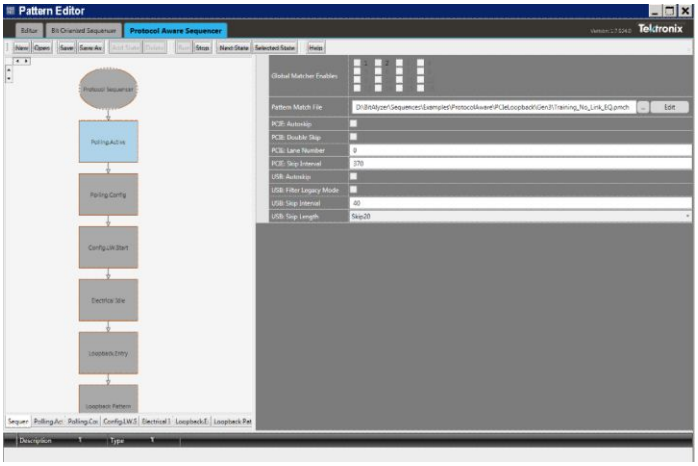
Pattern Sequencer editor

The BSX-series introduces a new pattern editor capable of supporting the bit-oriented and protocol-aware pattern as well as pattern sequence creation.



Sequence editor

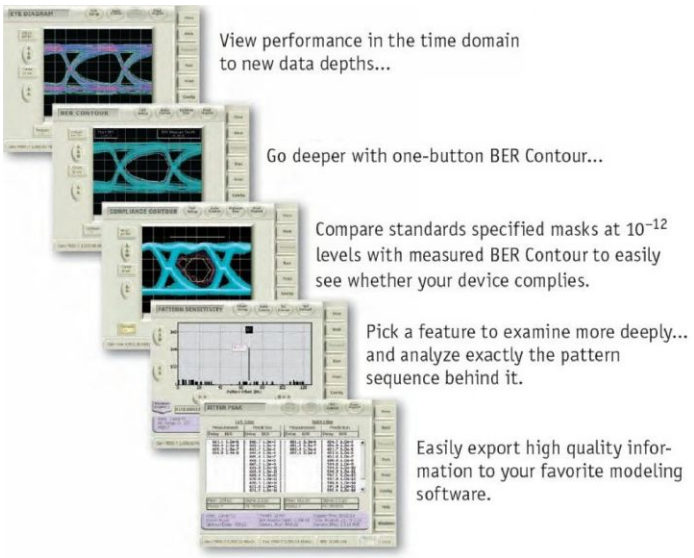
In Protocol Aware Sequencer mode, the editor translates the symbolic protocol messages to protocol-specific blocks of data (without any transformation) in the generator pattern memory. These blocks are then processed by the protocol-specific memory sequencer. This simplifies the generation of complex protocol data streams.



Sequencer

Linking domains

Eye diagrams have always provided an easy and intuitive view of digital performance. It has been harder to tie this directly with BER performance, as the instruments that provide views of each have been architected in fundamentally different ways. Eye diagrams have been composed of shallow amounts of data that have not easily uncovered rarer events. BERTs have counted every bit and so have provided measurements based on vastly deeper data sets, but have lacked the intuitive presentation of information to aid troubleshooting.



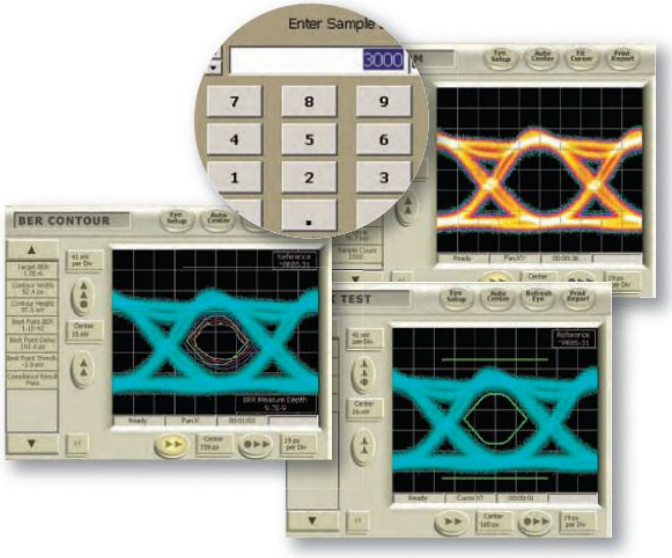
The BERTScope removes this gap allowing you to quickly and easily view an eye diagram based on at least two orders of magnitude more data than conventional eyes. Seeing a feature that looks out of the ordinary, you are able to place cursors on the item of interest and by simply moving the sampling point of the BERT, use the powerful error analysis capabilities to gain more insight into the feature of interest. For example, check for pattern sensitivity of the latest rising edges. Alternatively, use one-button measurement of BER Contour to see whether performance issues are bounded or likely to cause critical failures in the field. In each case, information is readily available to enhance modeling or aid troubleshooting, and is available for patterns up to 2^{31} - 1 PRBS.

Data rich eye diagrams

As shown previously, there is an impressive difference in data depth between conventional eye diagrams and those taken with a BERTScope. So what does that mean? It means that you see more of what is really going on - more of the world of low-probability events that is present every time you run a long pattern through a dispersive system of any kind, have random noise or random jitter from a VCO - a world that is waiting to catch you out when your design is deployed. Adding to this the deeper knowledge that comes from the one-button measurements of BER Contour, Jitter Peak, and Q-factor, and you can be confident that you are seeing the complete picture.

Deep mask testing

With the ability to vary sample depth, it is very easy to move between deep measurements which give a more accurate view of the real system performance, and shallow measurements that match those of a sampling oscilloscope. The measurements shown below are from the eye diagram of an optical transmitter. With the BERTScope sample depth set to only 3000 waveforms, the BERTScope generates the diagram shown in the middle in only 1 second. The measured mask margin of 20% exactly correlates to the same measurement made on a sampling oscilloscope. The lower diagram shows the eye produced by the same device, using Compliance Contour measured at a BER of 1×10^{-6}. Here the mask margin is reduced to 17%.



The depth advantage gained for eye diagrams is at least 10 times greater for mask testing. Unlike pseudo-mask testing offered by some BERTs, a BERTScope mask test samples every point on the perimeter of an industry-standard mask, including the regions above and below the eye. Not only that, but each point is tested to a depth unseen before. This means that even for a test lasting a few seconds using a mask from the library of standard masks or from a mask you have created yourself, you can be sure that your device has no lurking problems.

Accurate jitter testing to industry standards

Testing with long or short patterns, the most accurate jitter measurement is likely to come from the methodology that uses little or no extrapolation to get its result. With the BERTScope, you can quickly measure to levels of 1×10^{-9} (1×10-10 at high data rates), or wait for the instrument to measure 1×10^{-12} directly. Either way, the BERTScope's one-button measurements are compliant to the MJSQ jitter methodology, and because the underlying delay control is the best available on any BERT you can be sure that the measurements are accurate. Use the built-in calculations for Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ), or easily export the data and use your own favorite jitter model.

The BSX-series low intrinsic RJ supports serving of 802.3ba's simultaneous VECP (Vertical Eye Closure Penalty) and J2/J9 calibration with valuable margin required to fully characterize 100G Ethernet silicon.

Flexible clocking

The generator clock path features in the BERTScope provides the test flexibility needed for emerging real-world devices. Whether computer cards or disk drives, it is often necessary to be able to provide a sub-rate system clock, such as 100 MHz for PCI Express® (PCIe). To get the target card running may require a differential clock signal with a particular amplitude and offset; this is easily accomplished with the BERTScope architecture, with many flexible divide ratios available.

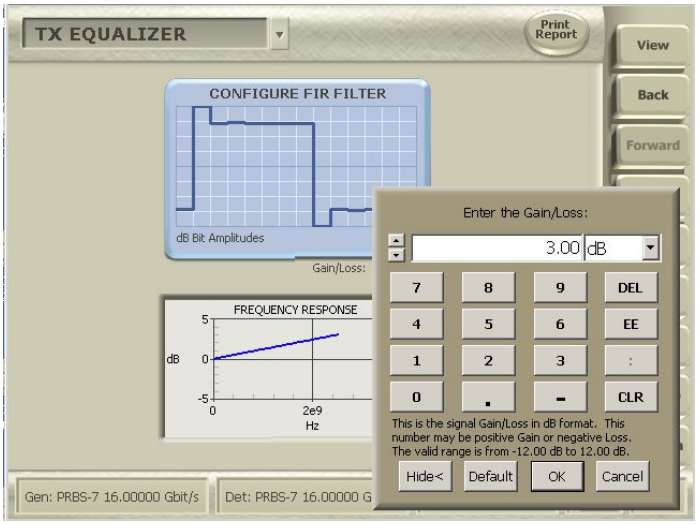
Spread Spectrum Clocking (SSC) is commonly used in electrical serial data systems to reduce EMI energy by dispersing the power spectrum. Adjustable modulation amplitude, frequency, and a choice of triangle or sine modulation wave shape allow testing receivers to any compliance standard which utilize SSC. An additional modulator and source allows users to stress the clock with high-amplitude, low-frequency Sinusoidal Jitter (SJ) at frequencies up to 4 MHz.

Programmable reference clock multiplier

To further add clocking flexibility, the BSX series provides a general purpose reference clock multiplier that allows the user to specify an integer clock multiplication ratio for an input reference clock frequency range of 10 MHz to 200 MHz. The clock output frequency is bounded by the frequency range of the clock synthesizer, which is 1 GHz to 16 GHz in the case of BSX series. Predefined multiplication ratios are included for many common standards.

Working with closed eyes

With the need to push ever-increasing data rates through electrical channels, the frequency-dependent losses often result in eye closure at the receiver end. Engineers use equalization to compensate for these losses and "open the eyes" in the real system. Tektronix offers powerful tools that allow designers to characterize and test compliance of receiver and transmitter components used in these systems.

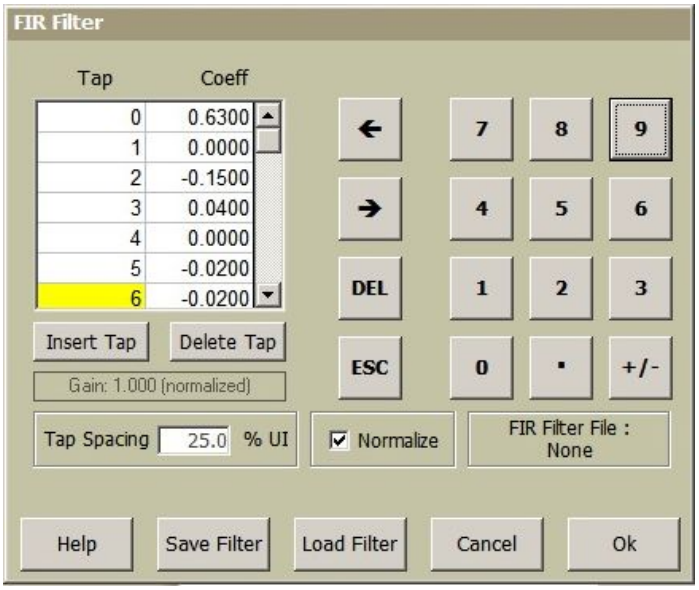


In keeping with the BERTScope philosophy, the graphical user interface presents the control functionality in a logical, easy-to-follow format. A time domain representation of the response shows the effects of tap weight settings. The frequency domain Bode plot shows how the filter will compensate for the channel losses.

For receiver testing, the BSX series included built-in 4-tap pre-emphasis/ de-emphasis capable of operation to the maximum data rate of the instrument, or 32 Gb/s in the case of the BSX320 model. Furthermore, fast control of output equalization supports link training response time requirements of the most stringent standards.

PatternVu

The PatternVu option includes a software-implemented FIR filter which can be inserted before the eye pattern display. In systems employing receiver equalization, this allows you to view the eye diagram and perform physical measurements on the eye as the receiver's detector would see it, after the effect of the equalizer. Equalizers with up to 32 taps can be implemented, and the user can select the tap resolution per UI.



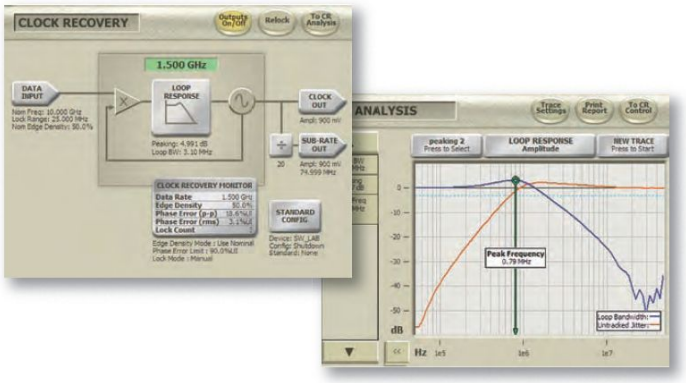
PatternVu

PatternVu also includes CleanEye, a pattern-locked averaging system which removes the nondeterministic jitter components from the eye. This allows you to clearly see pattern-dependent effects such as ISI (Inter-Symbol Interference) which are normally obscured by the presence of high amounts of random jitter.

Single Value Waveform export is a component in the PatternVu option. This allows you to capture a pattern-locked waveform showing single bits, similar to a single-shot capture in a real-time oscilloscope. Once captured, the waveform can be exported in a variety of formats for further analysis in an external program.

Add clock recovery

The Tektronix CR125A, CR175A, and CR286A add levels of flexibility in compliant clock recovery. Most standards requiring jitter measurement specify the use of clock recovery, and exactly which loop bandwidth must be used. Using a different or unknown loop bandwidth will almost certainly give you the wrong jitter measurement. The clock recovery instrument enables easy and accurate measurements to be made to all of the common standards.



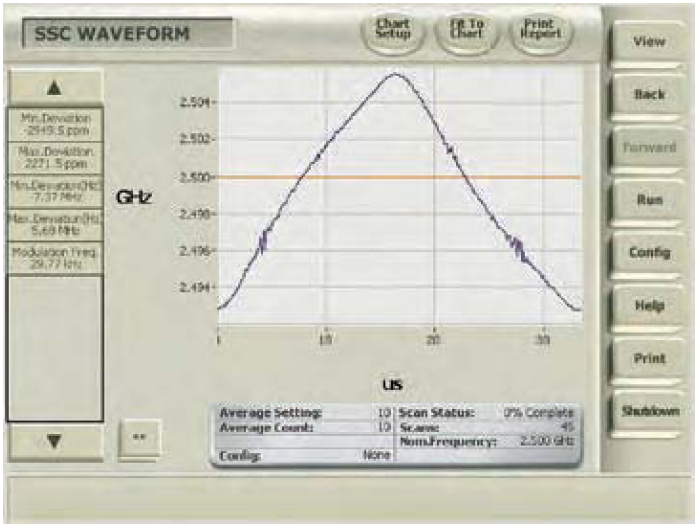
The intuitive user interface provides easy control of all operating parameters. A unique Loop Response view shows the loop characteristics – actually measured, not just the settings value.

The usefulness of the BERTScope CR is not just confined to BERTScope measurements. Use them stand-alone in the lab with your sampling oscilloscopes, or with existing BERT equipment. Compliant measurements are available to you by pairing either of these versatile instruments with your existing investments.

In addition, lock status and measured parameters such as pattern edge density and phase error are available on both the local built-in display and the BERTScope user interface for real-time views of input signal characteristics and CR performance.

Display and measure SSC modulation

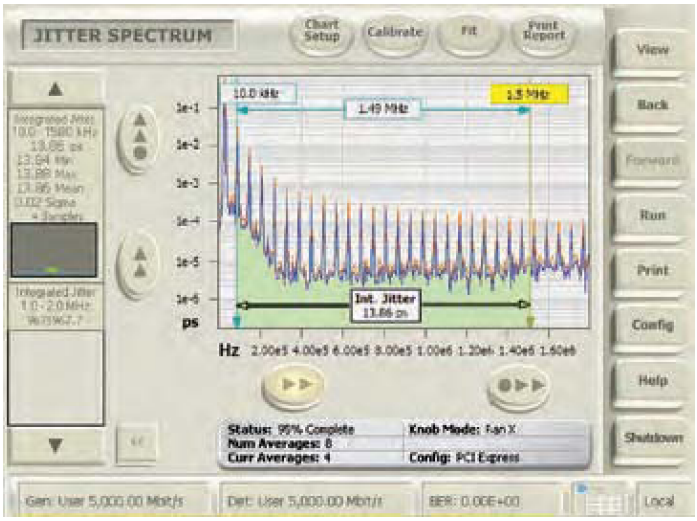
Spread Spectrum Clocking (SSC) is used by many of the latest serial busses including SATA, PCI Express, and SAS to reduce EMI issues in new board and system designs. The Tektronix CR Family provides spread spectrum clock recovery together with the display and measurement of the SSC modulation waveform. Automated measurements include minimum and maximum frequency deviation (in ppm or ps), modulation rate of change (dF/dT), and modulation frequency. Also included are display of the nominal data frequency and easy-to-use vertical and horizontal cursors.



SSC waveform measurement

Add jitter analysis

Combine a Tektronix CR125A, CR175A, or CR286A with Option 12GJ, 17GJ, and 28GJ respectively and your sampling oscilloscope or BERTScope for variable clock recovery from 1.2 to 11.2 Gb/s, Duty Cycle Distortion (DCD) measurement, and real-time jitter spectral analysis. Display jitter spectral components from 200 Hz to 90 MHz with cursor measurements of jitter and frequency. Measure band-limited integrated jitter with user-settable frequency-gated measurements (preset band limits and integrated jitter measurement for PCI Express 2.0 jitter spectrum in this example).

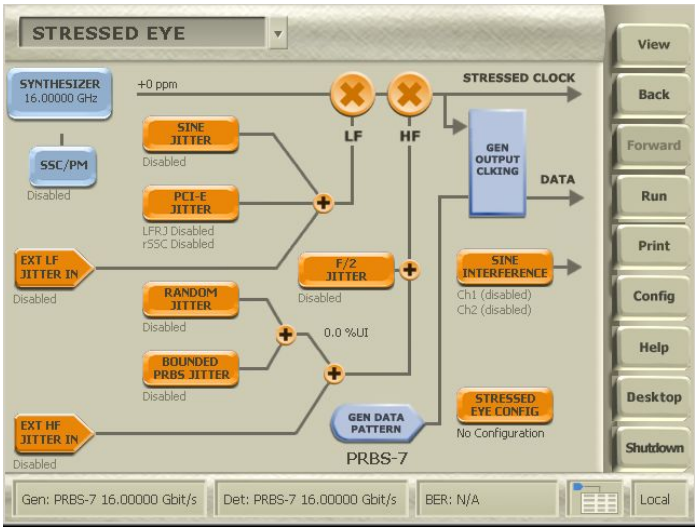


Jitter spectrum measurement

Taking stress out of receiver testing

As networks have changed, so have the challenges of testing receivers. While tests such as BER and receiver sensitivity are still important, receiver jitter tolerance has evolved to be more real-world for jitter-limited systems such as 10 Gb/s data over back planes and new high-speed buses. Stressed Eye testing is becoming increasingly common as a compliance measurement in many standards. In addition, engineers are using it to explore the limits of their receiver performance to check margins in design and manufacturing.

Creating the stress recipe for receiver testing to a complicated standard such as PCIe 2.0 used to require "racking and stacking" several instruments, then spending hours calibrating the setup. With BERTScope, an easy-to-understand graphical view gives you control of all of the calibrated stress sources you need – inside the same instrument. Eliminating the need for external cabling, mixers, couplers, modulators, etc. simplifies stress calibration.

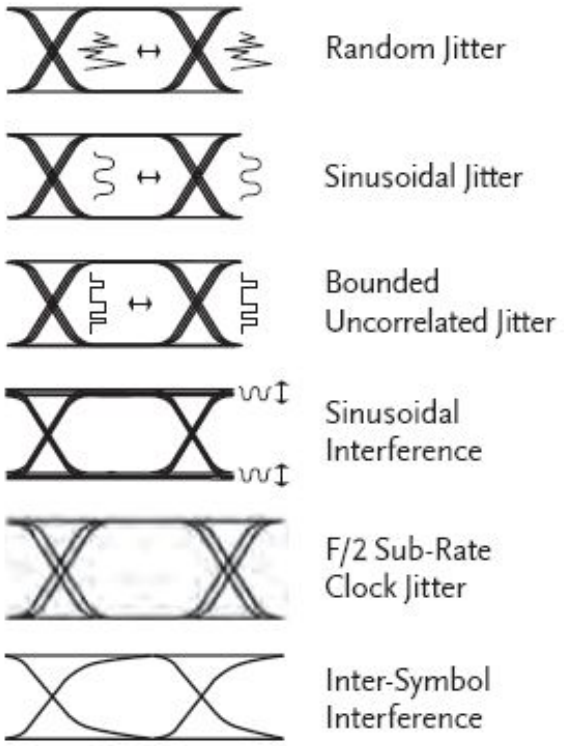


Stressed Eye view

Flexible stress impairments

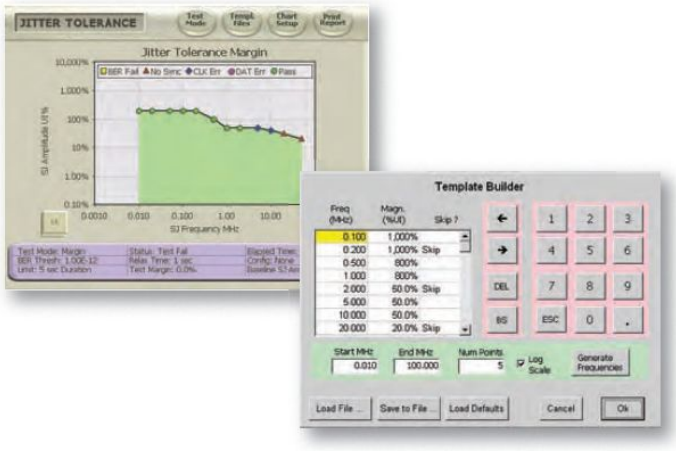
The BERTScope has high-quality, calibrated sources of stress built-in, including RJ, SJ, BUJ, and SI.

ISI is also a common ingredient in many standards. The BSA12500ISI differential ISI board provides a wide variety of path lengths, free from switching suck-outs and anomalies.



Flexible stress impairments

Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.



Built-in jitter tolerance function

BERTScope pattern generators

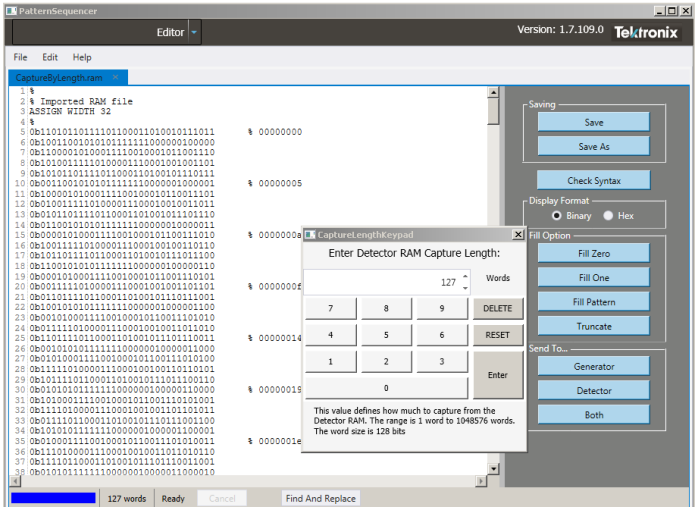
The BERTScope pattern generators provide a full range of PRBS patterns, common standards-based patterns, and user-defined patterns.

Option STR provides full integrated, calibrated stress generation which is an easy-to-use alternative to a rack full of manually calibrated instruments needed to provide a stressed pattern. Uses include receiver testing of devices with internal BER measurement ability such as DisplayPort, or adding stress capability to legacy BERT instruments.

Stressed eye option

Pattern capture

There are several methods for dealing with unknown incoming data. In addition to Live Data Analysis discussed above, a useful standard feature on all BERTScope analyzers is pattern capture. This allows the user to specify the length of a repeating pattern and then allow the analyzer to grab the specified incoming data using the detector's 512 Mb RAM memory. This can then be used as the new detector reference pattern, or edited and saved for later use.



Pattern capture

Pattern generator stressed eye

The pattern generator stressed eye function provides the following features:

- Flexible, integrated stressed eye impairment addition to the internal or an external clock
- Easy setup, with complexity hidden from the user with no loss of flexibility
- Verify compliance to multiple standards using the BERTScope and external ISI filters. Standards such as:
  - OIF CEI
  - 6 Gb SATA
  - PCI Express
  - XFI
  - USB 3.1
  - SONET
  - SAS
  - XAUI
  - 10 and 100 Gb Ethernet
  - DisplayPort
- Two sinusoidal interference sources are built into the BSX series BERTScope. These sources are summed internally, and are available as a single differential output on the front panel. When used with the optional external BSXCOMB kit, a variety of sinusoidal interference test configurations are supported, including the CM and DM interference requirements of PCIe Gen3 and Gen4.

Amplitude and ISI impairments

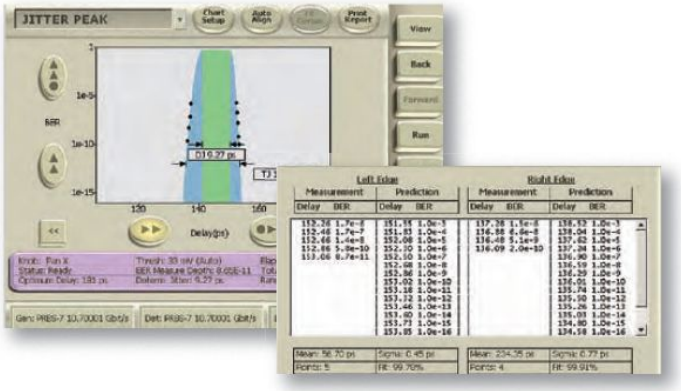
For ISI, add externally: for example, long coaxial cable length, or Bessel-Thompson 4th Order Filter with –3 dB point at 0.75 of bit rate, etc.

For applications requiring circuit board dispersion, the BSA12500ISI differential ISI accessory board can be used.

Jitter measurements

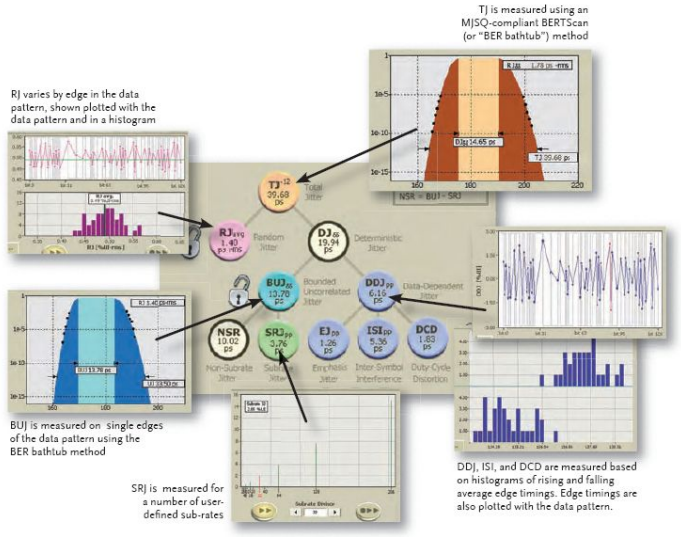
Multi-gigabit serial data channels have eye openings only a couple hundred picoseconds wide – or less. In systems where only a few picoseconds of jitter count, accurate measurement of jitter is essential for managing tight jitter budgets. The BERTScope has two sets of tools which perform these critical measurements.

The Physical Layer Test Suite option includes measurement of Total Jitter (TJ) along with breakdown into Random Jitter (RJ) and Deterministic Jitter (DJ), using the well-accepted Dual Dirac method. The deep, BERT-collected measurements use several orders of magnitude less extrapolation, or in some cases no extrapolation, than oscilloscopes use as a basis for the jitter measurements. This produces inherently more accurate results than measurements made on other instruments which rely on high levels of extrapolation.



MJSQ-compliant Dual Dirac jitter measurement.

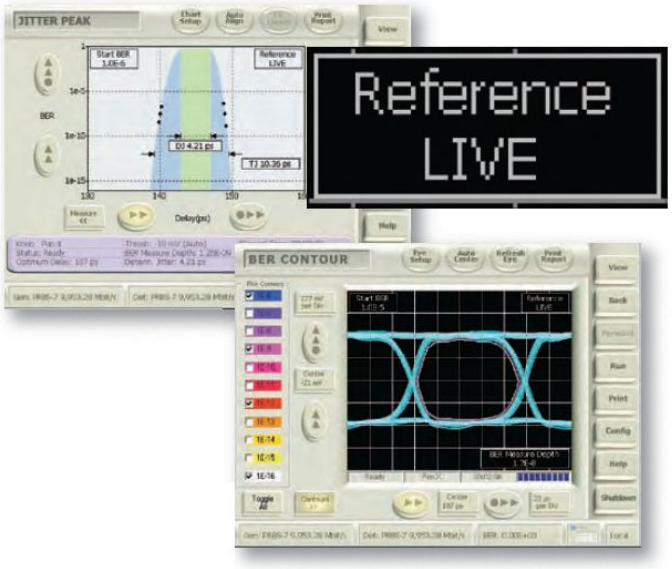
The optional Jitter Map is the latest suite of jitter measurements available for the BERTScope. It provides a comprehensive set of subcomponent analysis beyond RJ and DJ, including many measurements compliant with higher data rate standards. Jitter Map can also measure and decompose jitter on extremely long patterns, such as PRBS-31, as well as live data (requires Live Data Analysis option) providing that it can first run on a shorter synchronized data pattern.



Jitter map

Features include:

- DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) including F/2 (or F2) Jitter
- BER-based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10^{-12} BER and beyond
- Separation of correlated and non-correlated jitter components eliminates mistaking long pattern DDJ for RJ
- Can measure jitter with minimum eye opening
- Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data Dependent Pulse Width Shrinkage (DDPWS), and Non-ISI
- Intuitive, easy-to-navigate jitter tree



Jitter peak and BER contour measurements made on live data.

Flexible external jitter interfaces

Flexible external jitter interfaces include the following features:

- Front panel external high frequency jitter input connector – jitter from DC to 1.0 GHz up to 0.5 UI (max) can be added, of any type that keeps within amplitude and frequency boundaries
- Rear panel external SJ low frequency jitter input connector – jitter from DC to 100 MHz up to 1.1 ns (max) can be added
- Rear panel SJ output
- Sinusoidal interference output front panel connector

The internal RJ, BUJ, and external high-frequency jitter input is limited to 0.5 UI, combined, further limited to 0.25 UI each when both are enabled. Rear-panel low-frequency jitter input can be used to impose additional jitter; the sum of external low-frequency jitter, internal low-frequency SJ to 10 MHz, PCIe LFRJ and PCIe rSSC (with Option PCISTR) is limited to 1.1 ns. This limit does not apply to Phase Modulation (PM) from Option XSSC.

Jitter impairments

Bounded uncorrelated jitter:

- Supports data rates from 1.5 to 12.5 Gb/s (BSX125), 24 Gb/s (BSX240), and 32 Gb/s (BSX320)
- Internal PRBS Generator
- Variable up to 0.5 UI
- 100 Mb/s to 2.0 Gb/s
- Band-limited by selected filters

BUJ rate	Filter
100 to 499	25 MHz
500 to 999	50 MHz
1,000 to 1,999	100 MHz
2,000	200 MHz

Random jitter:

- Supports data rates from 1.5 to 12.5 Gb/s (BSX125), 24 Gb/s (BSX240), and 32 Gb/s (BSX320)
- Variable up to 0.5 UI
- Band-limited 10 MHz to 1 GHz; 1.5 MHz to 100 MHz in PCIe2 mode
- Crest factor of 16 (Gaussian to at least 8 standard deviation or about 1×10^{-16} probability)

Sinusoidal jitter

Modulation type	Internal SJ frequency	Maximum internal SJ amplitude
Phase modulation	10 Hz to 4 MHz	Up to 19200 UI ≥11.2 Gb/s
Low frequency SJ (selectable modulators [1])	1 kHz to 100 MHz	Up to 1000 ps < 22.4 Gb/s Up to 270 ps [2] 10 - 28.5 Gb/s Up to 130 ps 10 - 32 Gb/s
High frequency SJ	100 MHz to 1000 MHz	0.5 UI [3]

SJ adjustable from 0 to levels greater than or equal to range in table. Range is decreased at higher modulation rates and/or bit rates. See *Spread spectrum clock and phase modulation* for more PM capability detail and *Sinusoidal Jitter (SJ)* for more SJ capability detail.

Testing interface cards

Finally, a solution to the age-old problem of making physical layer measurements on high-speed line cards, motherboards, and live traffic – the BERTScope Live Data Analysis option. Through novel use of the dual-decision point architecture, the instrument is able to make parametric measurements such as Jitter, BER Contour, and Q-factor in addition to the eye and mask measurements that are usable as standard – all that is required is a clock signal. Add the Jitter Map option to see even more layers of jitter decomposition on live data. No more frustration because the pattern is not known, is unpredictable, or involves rate-matching word insertions. Troubleshooting is so much easier now that the one-button physical layer tests can be employed to provide unique insight.

1 Range is selectable between 1100 ps, 270 ps, and 130 ps maximum; a lower range has lower intrinsic jitter.

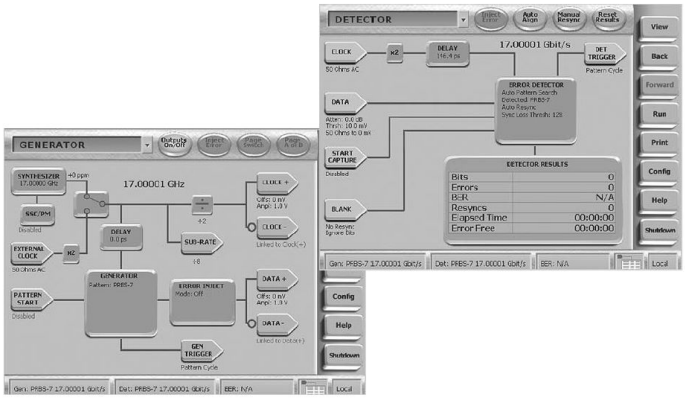
2 Full SJ range is 270 ps; with RJ or BUJ the range is reduced to 220 ps.

3 Total of HFSJ, BUJ, EXT HF jitter and RJ ≤ 0.5 UI total

User interfaces

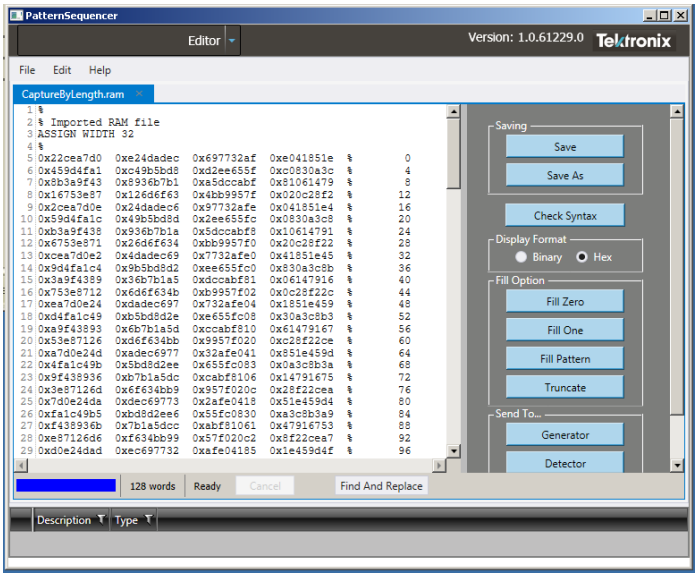
User interfaces take usability to new heights:

- Easy navigation
- Logical layout and operation
- Multiple ways of moving between screens
- Relevant information right where you need it
- Color coding to alert you to the presence of nonstandard conditions



UI setup screens

The pattern editor, pattern segment editor, and pattern sequencer are contained in a stand-alone view that requires a user supplied VGA-compatible monitor with minimum 1280 x 1024 resolution.



Pattern and sequence editor

Physical layer test view

The following physical layer test options are available:

- BER contour testing
  - Executed with same acquisition circuitry as eye diagram measurements for maximum correlation
  - As-needed delay calibration for accurate points
  - Automatic scaling, one-button measurement
  - Extrapolates contours from measured data, increasing measurement depth with run time and repeatedly updating curve fits
  - Easy export of fitted data in CSV format
  - Contours available from 10^{-6} to 10^{-16} in decade steps
- Basic jitter measurements
  - Testing to T11.2 MJSQ BERTScan methodology (also called ‘Bathtub Jitter’)
  - Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement
  - Separation of Random and Deterministic components, as defined in MJSQ
  - As-needed delay calibration for accurate points
  - Export of points in CSV format
  - Easy one-button measurement
  - User-specified amplitude threshold level, or automatic selection
  - Selectable starting BER to increase accuracy when using long patterns, as defined in MJSQ
- Q-factor measurement
  - One-button measurement of a vertical cross section through the middle of the eye
  - Easy visualization of system noise effects
  - Export of data in CSV format
- Compliance contour
  - Validation of transmitter eye performance to standards such as XFP/XFI and OIF CEI
  - Overlay compliance masks onto measured BER contours and easily see whether devices pass the BER performance level specified

Live data analysis option

The Live data analysis option is designed to measure parametric performance of traffic that is either unknown or non-repeating. This can include traffic with idle bits inserted, such as, in systems with clock rate matching. It is also suitable for probing line cards.

The option uses one of the two front-end decision circuits to decide whether each bit is a one or zero by placing it in the center of the eye. The other is then used to probe the periphery of the eye to judge parametric performance. This method is powerful for physical layer problems, but will not identify logical problems due to protocol issues, where a zero was sent when it was intended to be a one.

Live data measurements can be made using BER Contour, Jitter Peak, Jitter Map, and Q-factor. Eye diagram measurements can be made on live data without the use of this option, providing a synchronous clock is available.

The Live data analysis option requires the Physical layer test option and must be used with a full-rate clock.

PatternVu equalization processing option

PatternVu [4] adds several powerful processing functions to the BERTScope:

- CleanEye is an eye diagram display mode, which averages waveform data to present an eye diagram with the non-data-dependent jitter removed. This allows the user to view and measure data-dependent jitter such as Inter-Symbol Inference, giving an intuitive idea of the compensatable jitter present, for example. It is effective on any repeating pattern up to 32,768 bits long.
- Single value waveform export is a utility which converts the CleanEye output to an export file in Comma Separated Vector (CSV) format. The output file, of up to 105 bit points, can then be imported into Microsoft Excel or software analysis and simulation tools such as Stateye or MATLAB®. This allows offline filtering of real captured data and the implementation of standards-based processing such as Transmitter Waveform Dispersion Penalty (TWDP) required by 802.3aq, the recent Long Reach MultiMode (LRM) 10 Gb Ethernet standard.
- The FIR filter equalization processor allows the emulation of the communication channel to view and measure the eye as the detector in the receiver would, by applying a software linear filter to the data before it is displayed. For example, the FIR Filter can be used to emulate the lossy effects of a backplane channel, or alternatively, emulate the receiver's equalization filter, facilitating the design and characterization of receiver-side equalization.

  The filter characteristics are controlled by entering the individual weighting coefficients of a series of taps in the FIR filter. Up to 32 taps with tap spacing from 0.1 to 1.0 unit intervals (UI) can be programmed to allow fine resolution of the filter shape. The FIR Filter can be applied to repeating patterns up to 32,768 bits long.
- Single edge jitter measurement allows truly deep BER-based jitter measurements to be applied to individual data edges at data rates above 3 Gb/s. The Single Edge Jitter Peak measurement function enables computation of jitter on a user-selectable single edge in the pattern, for repeating patterns up to 32,768 bits long. The resulting jitter measurement excludes data-dependent effects, showing only the uncorrelated jitter components such as Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), and Periodic Jitter (PJ).
- Flexible measurements enable users to specify exactly the portion of the CleanEye waveform to use for accurate measurement of amplitude, rise and fall time, and de-emphasis ratio. Preprogrammed formulas for standards such as PCI Express and USB 3.1 are included.

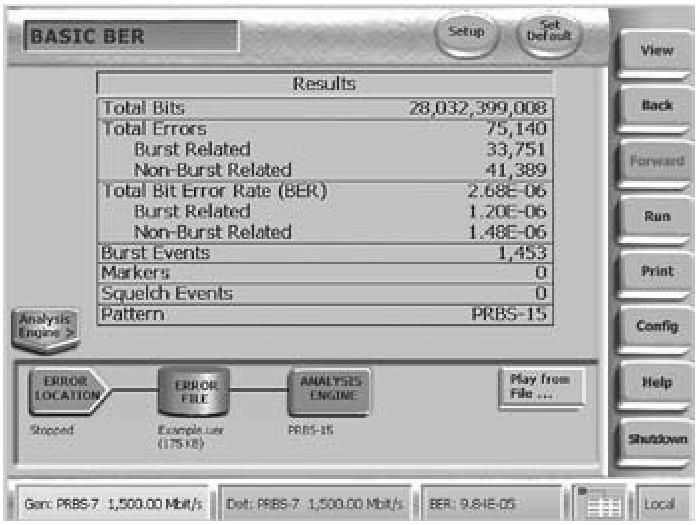
Error analysis

Error analysis is a powerful series of views that associate error occurrences so that underlying patterns can be easily seen. It is easy to focus in on a particular part of an eye diagram, move the sampling point of the BERTScope there, and then probe the pattern sensitivity occurring at that precise location. For example, it is straightforward to examine which patterns are responsible for late or early edges.

4 PatternVu operates at data rates of 900 Mb/s and higher.

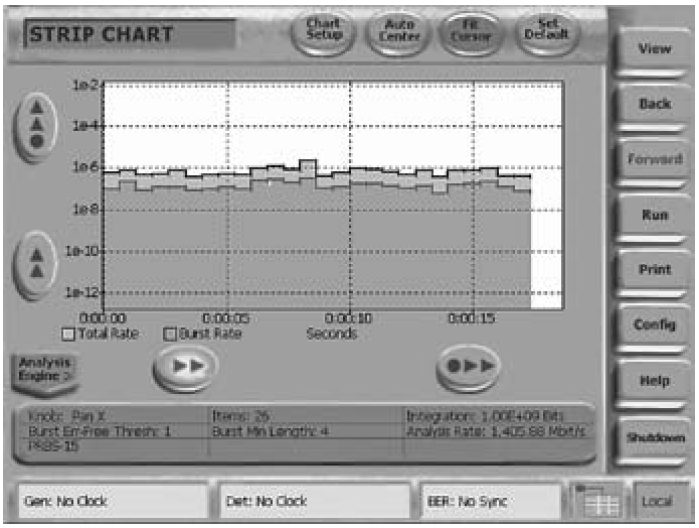
Many views come standard with the BERTScope Family:

- Error statistics: A tabular display of bit and burst error counts and rates



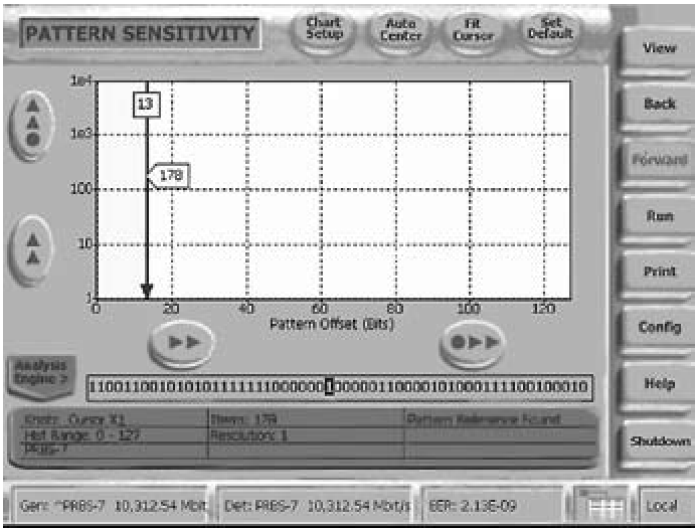
Error Statistics view showing link performance in terms of bit and burst occurrences.

- Strip chart: A strip chart graph of bit and burst error rates



Strip Chart view showing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting.

- Burst length: A histogram of the number of occurrences of errors of different lengths
- Error free interval: A histogram of the number of occurrences of different error-free intervals
- Correlation: A histogram showing how error locations correlate to user-set block sizes or external marker signal inputs
- Pattern sensitivity: A histogram of the number of errors at each position of the bit sequence used as the test pattern
- Block errors: A histogram showing the number of occurrences of data intervals (of a user-set block size) with varying numbers of errors in them



The Pattern Sensitivity view is a powerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns.

Forward error correction emulation option

Because of the patented error location ability of the BERTScope, it knows exactly where each error occurs during a test. By emulating the memory blocks typical of block error correcting codes such as Reed-Solomon architectures, bit error rate data from uncorrected data channels can be passed through hypothetical error correctors to find out what a proposed FEC approach would yield. Users can set up error correction strengths, interleave depths, and erasure capabilities to match popular hardware correction architectures.

2-D error mapping

This analysis creates a two-dimensional image of error locations from errors found during the test. Error mapping based on packet size or multiplexer width can show if errors are more prone to particular locations in the packet or particular bits in the parallel bus connected to the multiplexer. This visual tool allows for human eye correlation, which can often illuminate error correlations that are otherwise very difficult to find – even with all the other error analysis techniques.

Error location capture

Characteristic	Description
Live analysis	Continuous
Error logging capacity	Maximum 2 GB file size
Error events/second	10,000
Maximum burst length	32 kb

Jitter tolerance template

Many standards call for SJ to be stepped through a template with different SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps through a template that you designed, or one of the many standard templates in the library.

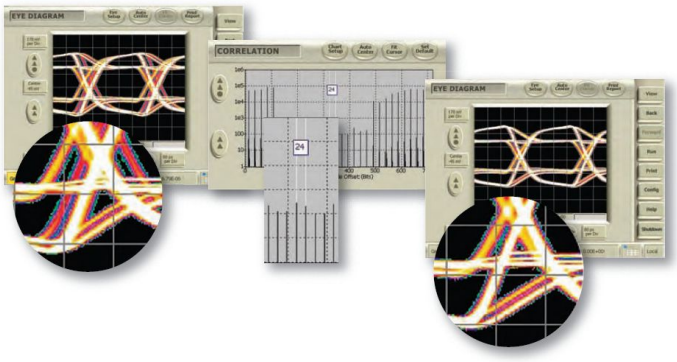
Some of the areas of adjustment include:

- BER confidence level
- Test duration per point
- BER threshold
- Test device relaxation time
- Imposition of percentage margin onto template
- Test precision Control over A/B Pattern switch behavior

Also included is the ability to test beyond the template to device failure at each chosen point, and the ability to export data either as screen images or CSV files.

Debugging with Error Location analysis

Using the Power of Error Analysis – In the following example eye diagram views were linked with BER to identify and solve a design issue in a memory chip controller. The eye diagram (top left) shows a feature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the system clock was at 1/24th of the output data rate. Redesigning the chip with greater clock path isolation gave the clean waveform of the top right eye diagram.



Power of error analysis example

Jitter map option

The Jitter map [5] option provides automated jitter decomposition with long pattern jitter triangulation. It extends BER-based jitter decomposition beyond Dual Dirac measurement of Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ) to a comprehensive set of subcomponents. It can also measure and decompose jitter on extremely long patterns, such as PRBS-31, providing that it can first run on a shorter synchronized data pattern.

The option includes the following features:

- DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) [6] including F/2 (or F2) jitter
- BER based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10^{-12} BER and beyond
- Separation of correlated and uncorrelated jitter components eliminates mistaking long pattern DDJ for RJ
- Visualization of RJ RMS measured on individual edges of the data pattern
- J2 and J9 jitter measurements for 100 GbE applications
- Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data Dependent Pulse Width Shrinkage (DDPWS), and non-ISI
- Intuitive, easy-to-navigate jitter tree

Stressed live data option

The BERTScope Stressed Live Data software option enables engineers to add various types of stress to real data traffic in order to stress devices with bit sequences representative of the environment they will encounter once deployed. Using live traffic with added stress tests the boundaries of device performance and lends added confidence to designs before they are shipped.

- Full range of calibrated stress available on the BERTScope, including Sinusoidal Jitter (SJ), Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), Sinusoidal Interference (SI), F/2 Jitter, and Spread Spectrum Clocking (SSC)
- Data rate support up to the maximum of the BERTScope
- Full-rate clock required up to 11.2 Gb/s, half-rate clock required above 11.2 Gb/s

5 Jitter map operates at data rates of 900 Mb/s and higher.

6 SRJ and F/2 jitter operate up to 11.2 Gb/s (all configurations)

Symbol filtering option

Symbol filtering enables asynchronous BER testing, including Jitter Tolerance testing, on incoming data streams that have a nondeterministic number of clock compensation symbols inserted into the bit stream, when placed in loopback for receiver testing.

- Supports asynchronous receiver testing for USB 3.1, SATA, SAS, and PCI Express
- User-specified symbols are automatically filtered from the incoming data to maintain synchronization.
- The Error Detector maintains a count of filtered bits for accurate BER measurement.

Pattern generator specifications

All specifications are guaranteed unless noted otherwise. All specifications apply to all models unless noted otherwise.

Rise times are measured 20% to 80% unless otherwise stated. Specifications are valid after a 20-minute warm-up period. Specifications are subject to change.

Data outputs

Data rate range	
BSX125	0.6 to 12.5 Gb/s
BSX240	1 to 24 Gb/s
BSX320	1 to 32 Gb/s
Format	NRZ
Polarity	Normal or inverted
Variable cross over	30 to 70%
Patterns	
Hardware patterns	Industry-standard Pseudo-random (PRBS) of the following types: 2^n - 1 where n = 7, 11, 15, 20, 23, 31
RAM patterns	128 bits to 512 Mbits total with support for 128 pattern sequencer states
Library	Wide variety including SONET/SDH, Fibre Channel based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more
Pattern sequencer	Implements indirect access to pattern memory
Modes	Bit mode – no protocol processing applied
	Protocol-aware mode – protocol processing applied for supported protocols
Sequencer states	Up to 128 pattern sequencer states
Loop levels	Two levels (up to 1 M iterations per loop)
Pattern segment size	Minimum 128 bits, single bit granularity up to maximum memory size.

Data outputs

Protocol mode	Operates in units of protocol blocks: For PCIe Gen3/Gen4, a single 128b/130b block For USB 3.1 SSP, a single128b/132b block For 8b/10b, from 1 to16 8b/10b symbols
Protocol processing	Protocol-aware mode processing includes: Packaging of symbols into protocol blocks Symbol encoding (8b/10b) Data scrambling (all protocols) DC balancing (PCIe Gen3/4, USB 3.1 SSP)

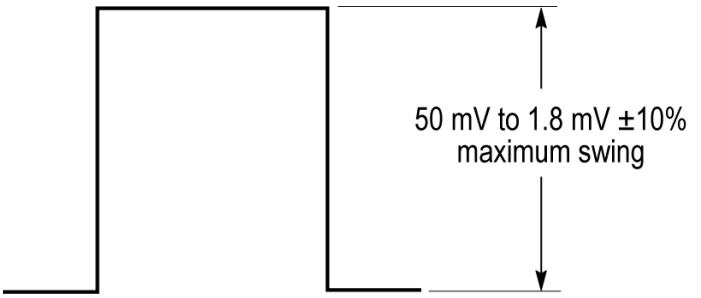
Error insertion	
Length	1, 2, 4, 8, 16, 32, 64 bit bursts
Frequency	Single or repetitive

Data output amplitudes and offsets

Configuration	Differential outputs, each side of pair individually settable for termination, amplitude, offset
Interface	DC coupled, 50 Ω reverse terminated, 3.5 mm connector. Calibration into 75 Ω selectable, other impedances by keypad entry. User-replaceable Planar Crown® adapter allows change to other connector types.
Preset logic families	LVPECL, LVDS, CML, ECL, SCFL

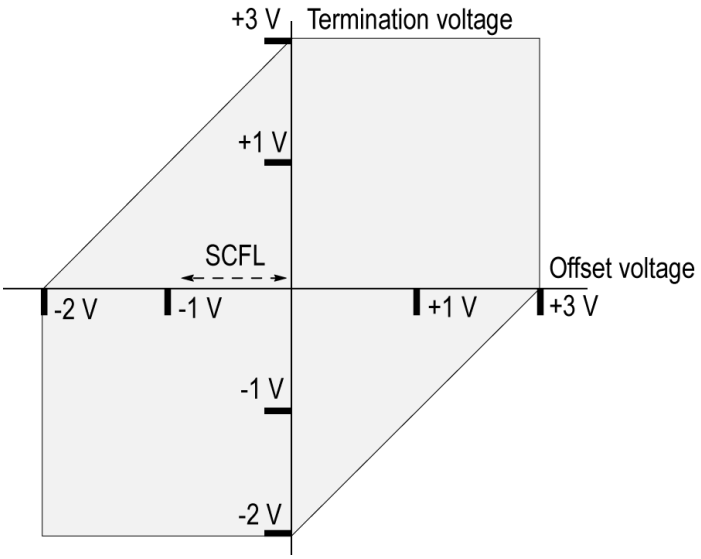
Data output amplitudes and offsets

Terminations	Variable, –2 to +3 V Presets: +1.5, +1.3, +1, 0, –2 V, AC coupled
Allowable amplitudes terminations and offsets	Refer to the following figures



Maximum swing

Amplitude swings between 0.050 and 1.8 V allowed; should fit inside shaded area of the following graph. For example, SCFL uses a 0 V termination, and operates between approximately 0 and –0.9 V; as shown with dotted arrow; it falls within the operating range.



Allowable amplitude and offset

Data output de-emphasis (Option TXEQ)

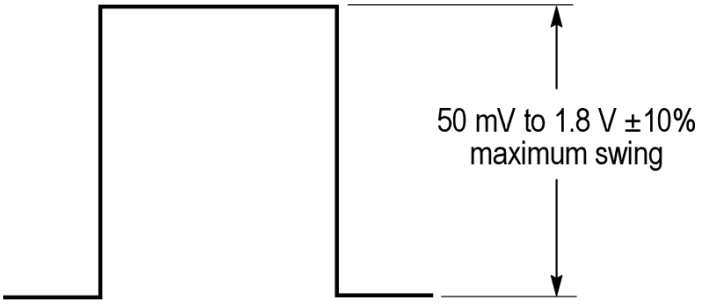
Data equalization type	4-Tap FIR Configured as 1 Pre-Cursor, 2 Post-Cursors
Data equalization tap range	Note: Sum of all cursors cannot exceed the Output Amplitude specification.
Pre-Cursor 1	±12 dB
Post-Cursor 1	±20 dB
Post-Cursor 2	±12 dB
Data equalization tap sign	±1; independent tap sign for all taps
Data equalization tap resolution	0.1 dB
Data equalization tap accuracy	±1 dB

Clock outputs

Frequency range	Maximum clock output frequency is half rate for bit rates ≥11.2 Gb/s.
BSX125	0.6 to 11.2 GHz
BSX240	1 to 12 GHz
BSX320	1 to 16 GHz
Phase noise	< –90 dBc/Hz at 10 kHz offset (typical)
Clock output divide ratios	Opt. STR only (See the Clock path details below.)

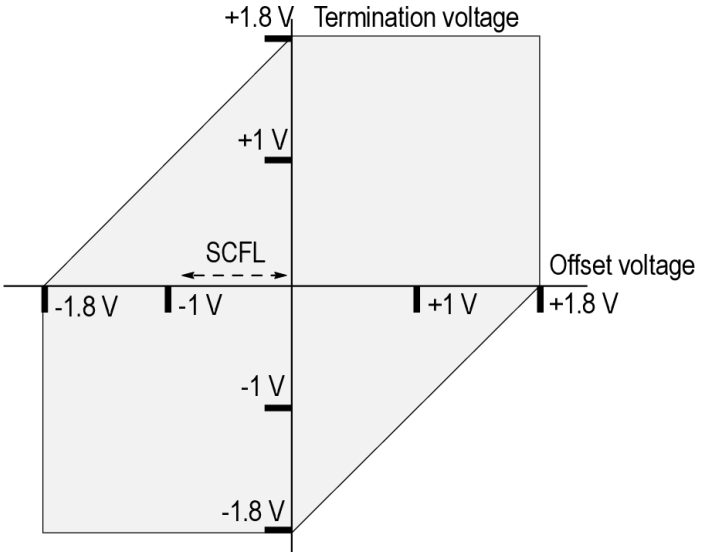
Clock output amplitudes and offsets

Configuration	Differential outputs, each side of pair individually settable for termination, amplitude, offset
Interface	DC coupled, 50 Ω reverse terminated, 3.5 mm connector. Calibration into 75 Ω selectable, other impedances by keypad entry. User-replaceable Planar Crown® adapter allows change to other connector types.
Preset logic families	LVPECL, LVDS, CML, ECL, SCFL
Terminations	Variable, –2 to +3 V Presets: +1.5, +1.3, +1, 0, –2 V, AC coupled
Allowable amplitudes, terminations, and offsets	Refer to the following figures



Maximum swing

Amplitude swings between 0.25 and 1.8 V allowed; should fit inside shaded area of the following graph. For example, SCFL uses a 0 V termination, and operates between approximately 0 and –0.9 V; as shown with dotted arrow, it falls within the operating range.



Allowable amplitude and offset

Data/clock waveform performance

Rise time	25 ps max, 23 ps typical (10-90%), 1 V amplitude, at 8.0 Gb/s
Jitter	
BSX125, BSX240	<500 fs RMS Random Jitter (@10.3125 Gb/s), typical
BSX320	≤8 ps_{p-p} TJ (@28.05 Gb/s), typical
	≤300 fs RMS Random Jitter (@28.05 Gb/s), typical

Clock/data delay

Range	Greater than 1 bit period in all cases
Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns
Resolution	100 fs
Self calibration	At time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

Pattern generator front panel connections

External clock input

Allows use of an external clock source to clock the BERTScope. Models equipped with stress are able to add impairments to incoming clock, including when external signal has Spread Spectrum Clocking (SSC) in excess of 5000 ppm imposed on it.

Frequency range	
BSX125	0.6 to 12.5 GHz
BSX240	1 to 24 GHz
BSX320	1 to 32 GHz
Nominal power	0 dBm
Maximum power	2.0 V_{p-p} (+10 dBm)
Return loss	Better than –6 dB
Interface	50 Ω SMA female, DC coupled into selectable termination voltage

HF Jitter (Option STR only)

One of two jitter insertion inputs. Can be used to insert SJ, RJ, BUJ if desired.

Frequency range	DC to 1.0 GHz
Jitter amplitude range	Up to 0.5 UI maximum
Input voltage range	0-2 V_{p-p} (+10 dBm) for normal operation
	6.3 V_{p-p} (+20 dBm) max nondestructive input

HF Jitter (Option STR only)

Data rate range

BSX125	1.5 to 12.5 Gb/s
BSX240	1.5 to 24 Gb/s
BSX320	1.5 to 32 Gb/s

Interface SMA female, 50 Ω, DC coupled into 0 V

Sub-rate clock outputs

BERTScope standard models have clock divided by 4. BERTScope Option STR models have additional capabilities.

Multi-rate and subrate divider ratios for main clock out with option STR

Data rate (Gb/s)	Ratios for main clock output	Ratios for sub-rate clock output [7]
600-750 Mb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 32, 36	1, 2, 4
0.75-3 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 144, 162	1, 2, 4, 8
3-6 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 216, 224, 252, 256, 288, 324	1, 2, 4, 8, 16, 32
6-11.2 Gb/s	1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 30, 32, 32, 35, 36, 36, 40, 42, 45, 48, 50, 54, 56, 60, 64, 70, 72, 80, 81, 84, 90, 98, 108, 112, 126, 128, 140, 144, 144, 160, 162, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 360, 384, 392, 432, 448, 504, 512, 576, 648	1, 2, 4, 8, 16, 32, 64
11.2-12 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648	2, 4, 8, 16, 32, 64
12-32 Gb/s	2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 60, 64, 64, 70, 72, 72, 80, 84, 90, 96, 100, 108, 112, 120, 128, 140, 144, 160, 162, 168, 180, 196, 216, 224, 252, 256, 280, 288, 288, 320, 324, 324, 336, 360, 384, 392, 400, 432, 448, 480, 504, 512, 560, 576, 640, 648, 720, 768, 784, 864, 896, 1008, 1024, 1152, 1296	2, 4, 8, 16, 32, 64, 128

Amplitude range 0.6 V_{p-p}, nominal, centered around 0 V

Transition time <500 ps

Interface SMA female, 50 Ω, DC coupled into 0 V

7 Sub-rate clock connector can also output a full-rate stressed clock up to 11.2 Gb/s, or half-rate stressed clock at rates ≥11.2 Gb/s.

Trigger output

Provides a pulse trigger to external test equipment. It has two modes:

- Divided Clock Mode: Pulses at 1/256th of the clock rate
- Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Stress modulation added on models so equipped, when enabled.

Minimum pulse width	128 Clock Periods (Mode 1) 512 Clock Periods (Mode 2)
Transition time	<500 ps
Jitter (p-p, data to trigger)	<10 ps, typical
Output levels	CML; >300 mV_{p-p}, center around -250 mV
Interface	50 Ω SMA female

Sine interference outputs

The SINE INTERFERENCE OUT+ and - outputs provide mixed sinusoidal signals for use in creating level interference. Two internal interference channels are provided and each is selectable to be in phase or out of phase at the two front panel outputs. Signals may be combined externally with the BSX data outputs to provide common mode (CM) and differential mode (DM) interference using the optional BSXCOMB kit.

Frequency range	2 MHz to 6000 MHz
Amplitude [8]	
SINE INTERFERENCE OUT +	0 to 2000 mV (Sum of Channel 1 and Channel 2 amplitudes)
SINE INTERFERENCE OUT -	0 to 2000 mV (Sum of Channel 1 and Channel 2 amplitudes)
Mode selection	
Channel 1	In-Phase, Out-of-Phase, Single-Ended (to SINE INTERFERENCE OUT + only)
Channel 2	In-Phase, Out-of-Phase, Single-Ended (to SINE INTERFERENCE OUT - only)
Interface	50 Ω differential, SMA female, (DC coupled into 0 V)

Pattern generator rear panel connections

Pattern start input

For users wanting to synchronize patterns of multiple data streams from multiple instruments simultaneously.

Logic levels	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V, typical
Maximum nondestructive input range	–0.5 V to +5.0 V
Minimum pulse width	128 serial clock periods

8 When used with external combiner BSXCOMB, added interference is total amplitude divided by five.

Pattern start input

Maximum repetition rate	512 serial clock periods
Interface	SMA female, >1 kΩ impedance into 0 V

Page Sel (Sequencer advance)

Allows external control of pattern sequencer state advance. Software control over rising and falling edge trigger.

Logic levels	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V, typical
Maximum nondestructive input range	–0.5 V to +5.0 V
Minimum pulse width	One pattern length
Interface	SMA female, >1 kΩ impedance into 0 V

Low frequency jitter input (Option STR only)

The LF JIT IN input allows use of an external low-frequency jitter source to modulate the stressed Pattern Generator output.

Frequency range	DC to 100 MHz
Jitter amplitude range	Up to 1.1 ns; can be combined with other internal low-frequency modulation
Input voltage range	0-2 V_{p-p} (+10 dBm) for normal operation 6.3 V_{p-p} (+20 dBm) maximum nondestructive input
Data rate range	
BSX125	Up to 12.5 Gb/s
BSX240	Up to 24 Gb/s
BSX320	Up to 32 Gb/s
Interface	SMA female 50 Ω, DC coupled into 0 V

Low frequency sinusoidal jitter output (Option STR only)

The LF SIN OUT output allows phasing the SJ of two BERTScopes together, in-phase or anti-phase.

Frequency range	As set for internal SJ from user interface
Amplitude	2 V_{p-p}, centered at 0 V
Interface	50 Ω SMA female, AC coupled

Reference input

To lock the BERTScope to an external frequency reference from of another piece of equipment.

Frequency	
Clock Synthesizer mode	10 MHz, 100 MHz, 106.25 MHz, 133.33 MHz, 156.25 MHz, 166.67 MHz, or 200 MHz
Ref Clock Multiplier mode	10 MHz to 200 MHz
Amplitude	0.325 to 1.25 V_{p-p} (–6 to +6 dBm)
Interface	50 Ω SMA female, AC coupled

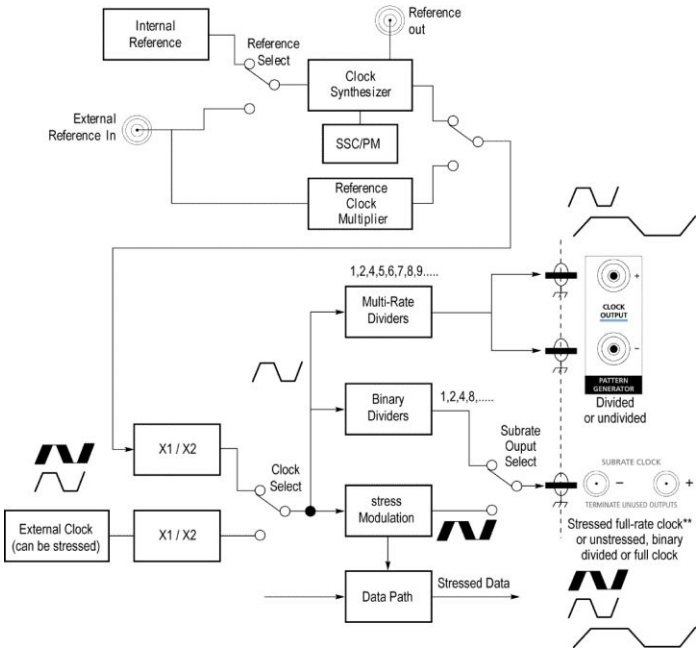
Reference output

Provides a frequency reference for other instruments to lock to

Configuration	Differential
Frequency	10 MHz, 100 MHz, 106.25 MHz, 133.33 MHz, 156.25 MHz, 166.67 MHz, or 200 MHz
Amplitude	1 V_{p-p} (+4 dBm) nominal, each output, (2 V_{p-p} differential)
Interface	50 Ω SMA female, AC coupled

Pattern generator clock path

BSX series clock path details



Functional block diagram of the clock path for models with stress capability.

** Stress may be added to an external clock on appropriate models. Stress operating range is from 1.5 to 11.2 Gb/s. External clock must have a duty cycle of 50% ±2%.

The BSX series BERTScope models use an internal Double Data Rate (DDR) architecture to operate at data rates ≥11.2 Gb/s. When operating at 11.2 Gb/s or higher data rate, the clock output will be 1/2 the data rate. The external clock can be specified to be either full or half data rate. When full rate is selected, the pattern generator will operate in DDR mode when the input clock frequency is 11.2 GHz or higher.

These ratios apply to operation from internal clock only. The external clock will be output at 1/2 rate when half rate is selected, or when full rate is selected and clock rate is ≥11.2 GHz.

The minimum data rate specified for the main clock output is 600 Mb/s for model BSX125 or 1 Gb/s for models BSX240 and BSX320. The output will be uncalibrated when operated at divided rates lower than the minimum specified data rate.

Reference clock multiplier

The Reference Clock Multiplier (RCM) is a phase locked loop (PLL) that produces the generator clock by frequency multiplying the signal entering the REF IN input on the rear panel. For best performance, a low jitter signal with a fast slew rate and amplitude near the REF IN maximum is recommended as the input reference.

Reference clock multiplier

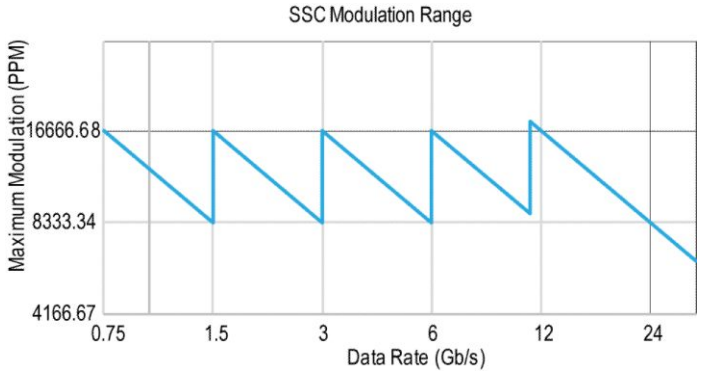
Supported standards

The following table lists the parameters of each supported standard, including the typical bandwidth and peaking of the RCM when the standard is selected.

Standard	Ref Clk input (MHz)	Multiplier	Data rate (Gbps)	PLL Loop Bandwidth (MHz, Typical)	Peaking (dB, Typical)
PCIe 4	100	160	16	3.5	1.5
PCIe 3	100	80	8	3.5	1.5
PCIe 2	100	50	5	5.5	0.75
PCIe 1	100	25	2.5	5	2
SD UHS-II Gen 2	52 to 104	30	1.56 to 3.12	2	1.5
SD UHS-II Gen 2	52 to 104	60	3.12 to 6.24	2	1.5
MIPI M-PHY	19.2 [9]	65/76/130/ 152/260/304	1.248/1.4592/2.496/ 2.9184/4.992/5.8368	2	1.5
	26	48/56/96/ 112/192/224	1.248/1.456/2.496/ 2.912/4.992/5.824	2	1.5
	38.4	32.5/38/65/ 76/130/152	1.248/1.4592/2.496/ 2.9184/4.992/5.8368	2	1.5
	52	24/28/48/ 56/96/112	1.248/1.456/2.496/ 2.912/4.992/5.824	2	1.5
General purpose	10 to 200	Any integer	1 to 32 [10]	0.15	1.5

SSC Tolerance

When any standard other than General Purpose is selected, the Reference Clock Multiplier is designed to tolerate the presence of Spread Spectrum Clocking (SSC) on the REF IN input. The SSC can be Up Spread, Center Spread, or Down Spread. For SSC frequencies between 20 and 40 kHz, the maximum amount of SSC the RCM can typically tolerate is as shown in the following graph.



9 REFIN should be 50% duty cycle for MIPI M-PHY 19.2 and 26 MHz references.

10 Data rate shown is for the BSX320. The BSX125 range is 0.6 to 12.5 Gb/s; the BSX240 range is 1 to 24 Gb/s.

Stress capabilities

Sinusoidal Jitter (SJ)

Operating bit rate	SJ amplitude is dependent on bit rate and modulation frequency.
BSX125	1.5 Gb/s to 12.5 Gb/s
BSX240	1.5 Gb/s to 24.0 Gb/s
BSX320	1.5 Gb/s to 32.0 Gb/s
Minimum modulation frequency	1 kHz
Maximum modulation frequency	100 MHz
Modulation frequency resolution	100 Hz
Maximum modulation amplitude	
1100 ps range	1100 ps < 22.4 Gb/s with SJ frequency ≤ 1 MHz
	900 ps ≤ 22.4 Gb/s with SJ frequency = 10 MHz
	400 ps ≤ 22.4 Gb/s with SJ frequency = 40 MHz
	100 ps ≤ 22.4 Gb/s with SJ frequency = 100 MHz
270 ps range[11]	270 ps ≥ 10 and ≤ 28.5 Gb/s with SJ frequency ≤ 40 MHz
	260 ps ≥ 10 and ≤ 28.5 Gb/s with SJ frequency > 40 MHz, ≤ 80 MHz
	250 ps ≥ 10 and < 28.5 Gb/s and SJ frequency > 80 MHz, ≤ 100 MHz
130 ps range	130 ps ≥ 10 and ≤ 32 Gb/s with SJ frequency ≤ 100 MHz

Bounded Uncorrelated Jitter (BUJ)

Operating bit rate	
BSX125	1.5 Gb/s to 12.5 Gb/s
BSX240	1.5 Gb/s to 24.0 Gb/s
BSX320	1.5 Gb/s to 32.0 Gb/s
Minimum modulation frequency	100 MHz
Maximum modulation frequency	2000 MHz
Modulation frequency resolution	100 kHz
Maximum modulation amplitude	0.5 UI
	Total of EXT HF Jitter, BUJ, HFSJ, and RJ must be less than 0.5 UI
Modulation pattern	PN7

11 Range of the 270 ps modulator is reduced by 50 ps when HFSJ, BUJ, EXT HF Jitter or RJ is enabled.

Bounded Uncorrelated Jitter (BUJ)

Pattern filter

Bit rate (Mb/s)	Filter bandwidth (MHz)
100 to 499	25
500 to 999	50
1000 to 1999	100
2000	200

Random Jitter (RJ)

Operating bit rate

- **BSX125** 1.5 Gb/s to 12.5 Gb/s
- **BSX240** 1.5 Gb/s to 24.0 Gb/s
- **BSX320** 1.5 Gb/s to 32.0 Gb/s

Minimum modulation spectrum
10 MHz Standard mode
1.5 MHz PCIe2 mode

Maximum modulation spectrum
1000 MHz Standard mode
100 MHz PCIe2 mode

Maximum modulation amplitude
0.5 UI
Total of EXT HF Jitter, BUJ, and RJ must be less than 0.5 UI.

Crest factor 16

High Frequency SJ (HFSJ)

Operating bit rate

- **BSX125** 1.5 Gb/s to 12.5 Gb/s
- **BSX240** 1.5 Gb/s to 24.0 Gb/s
- **BSX320** 1.5 Gb/s to 32.0 Gb/s

Minimum modulation frequency 100 MHz

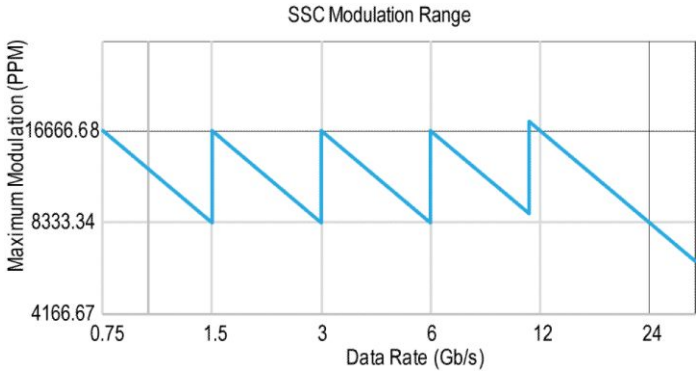
Maximum modulation frequency 1000 MHz

Maximum modulation amplitude
0.5 UI
Total of EXT HF Jitter, BUJ, HFSJ, and RJ must be less than 0.5 dB.

Spread spectrum clock and phase modulation

Modulates the synthesizer clock output – modulation affects main and sub-rate clock outputs (regardless of the state of sub-rate output select), Data Output, and Trigger Output.

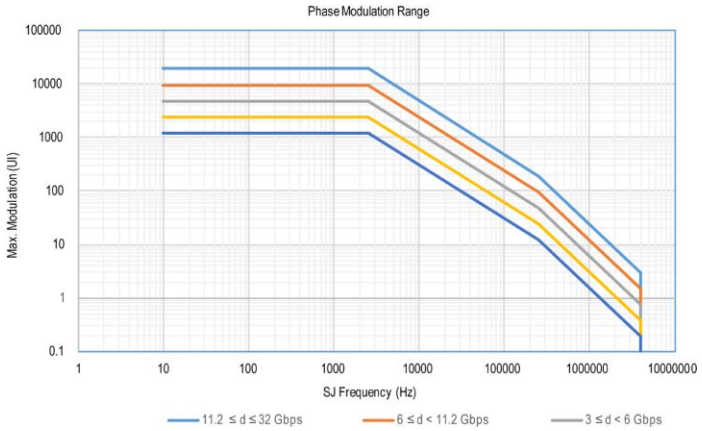
Modes	SSC, Phase Modulation (sinusoidal)
Data rate range	Full range of BERTScope
SSC wave shape	Triangle or Sine
SSC frequency range	20 kHz to 40 kHz
SSC modulation range	16,666 ppm at 6 Gb/s and 12 Gb/s 12,500 ppm at 8 Gb/s and 16 Gb/s See Maximum SSC Modulation graph for range vs. data rate
SSC modulation resolution	1 ppm
SSC modulation type	Down Spread, Center Spread, Up Spread
PM frequency range	10 Hz to 4 MHz
PM frequency resolution	1 Hz



Spread spectrum clock and phase modulation

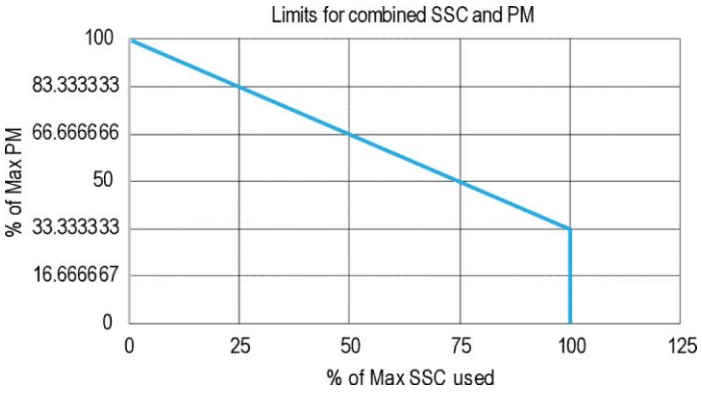
PM modulation range -- for modulation frequency 10 Hz to 2.5 kHz

Data rate (d)	Maximum modulation
11.2 ≤ d ≤ 32 Gbps	19200 UI
6 ≤ d < 11.2 Gbps	9600 UI
3 ≤ d < 6 Gbps	4800 UI
1.5 ≤ d < 3 Gbps	2400 UI
0.75 ≤ d < 1.5 Gbps	1200 UI
Reduced for modulation frequencies >2.5 kHz	See Phase Modulation Range graph.



Combined SSC and PM Limits

See the following graph, referenced to the maximum SSC and PM limits identified in previous table.



F/2 jitter generation option (Option F2, also requires Option STR)

F/2 or sub-rate jitter is found in high data rate systems which multiplex up 2 or more lower data rate streams. The jitter results for lack of symmetry in the multiplexing clock, giving all of the even bits different pulse width than the odd bits. Unlike conventional DCD, F/2 jitter is independent of the logic state of the bit. F/2 jitter is part of the stress recipe used in testing compliance to some of the standards such as 802.3ap (10 Gb backplane Ethernet).

Supported data rates	8.0 and 10.3125 Gb/s
Modulation range	0-5.0% UI

Extended stress generation

Adds additional stress generators required for compliance testing receivers to PCIe 2.0 specifications, internal to the BERTScope.

Clock frequency range	Up to 22.4 Gb/s
LFRJ modulation range	0 to 1.1 ns [12]
LFRJ frequency range	Band-limited to 10 kHz - 1.5 MHz, with roll off to PCIe 2.0 specifications
rSSC modulation range	0 to 368 ps [13] at 5 Gb/s
rSSC frequency range	1 to 35 kHz
Selectable bandwidth	Extended Stress adds selectable bandwidth-limiting to the normal, broadband RJ generator.
RJ frequency normal mode	Band-limited to 10 MHz to 1 GHz
RJ frequency PCIE mode	Band-limited to 1.5 to 100 MHz with roll off to PCIe 2.0 specifications

12 Limit applies when the 1100 ps modulator is used. Range is reduced if a different modulator is selected.

13 Can be combined with other low-frequency modulation.

Error detector specifications

Clock input

Configuration	Single ended
Frequency range	
BSX125	0.6 to 12.5 Gb/s
BSX240	1 to 24 Gb/s
BSX320	1 to 32 Gb/s [14]

Data and clock interfaces

Connector	3.5 mm
Impedance	50 Ω
Threshold voltage	–2 to +3.5 V
Threshold presets	LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations	Variable, –2 V to +3 V Presets: +1.5, +1.3, +1, 0, –2 V, AC coupled
Maximum nondestructable input	–3 V_{Peak}, +4 V_{Peak}, applied to any connector

Detector clock data delay

Range	Greater than 1 bit period in all cases
Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns
Resolution	100 fs
Self calibration	Supported – At time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

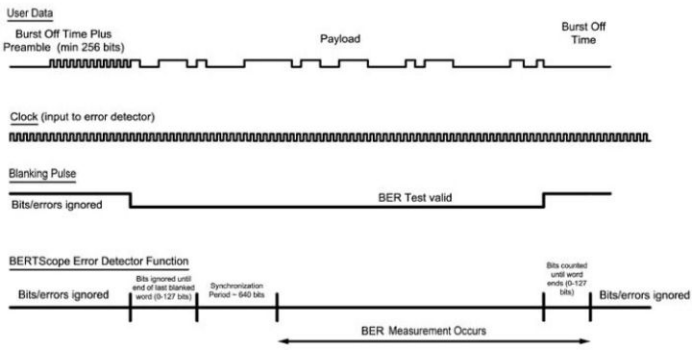
Data inputs

Data rate range	
BSX125	0.5 to 12.5 Gb/s
BSX240	1 to 24 Gb/s
BSX320	1 to 32 Gb/s
Configuration	Differential
Format	NRZ
Polarity	Normal or inverted

14 13 From 26 to 32 Gb/s the input detector operates at half rate (using even or odd bits)

Data inputs

Threshold alignment	Can auto-align to differential crossing point
Sensitivity	
Single-ended	100 mV_{p-p}, typical
Differential	50 mV_{p-p}, typical
Maximum input signal swing	2 V_{p-p}
Intrinsic transition time	16 ps typical, 10/90%, single ended (equivalent to >20 GHz detector bandwidth). Measured at input, ECL levels
Hardware patterns	Industry-standard Pseudo-random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31
RAM patterns	
User defined	128 bits to 512 Mb, 1-bit increments
Library	Wide variety including SONET/SDH, Fibre Channel based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more
RAM pattern capture	Capture incoming data up to 512 Mb in length. Edit captured data, send to Pattern Generator, Error Detector, or both
RAM pattern capture modes	
Capture by length	Captures to Detector pattern memory when Capture Length is selected.
Capture by triggers	Captures when “Detector Start” on rear panel goes high, to maximum allowable length or until input goes low
Capture by length from trigger	Capture by length initiated from “Detector Start” input, to pre-specified length
Detector pattern match	Optional user defined detector pattern matching used to advance pattern generator sequencer state and creating event-based triggers. Allows the user to create their own link state traversals via stimulus-response feedback (protocol handshaking)
Modes	Bit Oriented Sequencer mode – no protocol processing applied
	Protocol Aware Sequencer mode – protocol processing applied for supported protocols
Bit mode	Four, general-purpose pattern matchers available. Will find any arbitrary pattern up to 128 bits in length in incoming data stream, with bit masking available
Protocol Aware Sequencer mode	Sixteen pattern match elements are available in Detector for protocol-based pattern matching
	PCIe Gen3/4, USB 3.1 SSP: can match entire decoded block payload, with bit/byte masking
	8b/10b: can match up to 16 8-bit symbols after block/symbol decoding, with masking
Synchronization - Auto resync	User-specified number of 128 bit words containing 1 or more errors per word initiates a re-sync attempt



BERTScope Burst Analysis Timing – BERTScope word size is 128 bits. An example timing diagram is shown here for a PRBS payload. Counting of bits will not start until a 128-bit word boundary occurs, meaning that after the blanking pulse transitions, up to 127 bits may pass before synchronization begins. For a PRBS, synchronization typically takes 5 words, or 640 bits. Similarly, bit measurement will continue for up to 127 bits after the blanking signal transitions again. RAM-based patterns take longer to synchronize.

Data inputs

Manual synchronization	User initiates re-sync
Pattern matching synchronization	
Grab 'n' go	Error Detector captures specified pattern length and compares next instances to find match (Fast method, but susceptible to ignoring logical errors).
Shift-to-sync	Error Detector compares incoming pattern with reference RAM pattern, looks for match, if none found shifts pattern by one bit and compares again (slower, but most accurate method).
Error detector basic measurements	BER, Bits Received, Re-syncs, Measured Pattern Generator and Error Detector Clock Frequencies

Error detector front panel connections

Blank input

Useful for recirculating loop fiber experiments or during channel training sequences. Causes errors to be ignored when active. Bit count, error count, and BER not counted. No re-sync occurs when counting is re-enabled.

Logic family	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 clock periods
Maximum repetition rate	512 serial clock periods
Interface	SMA female, >1 kΩ impedance into 0 V

Error output

Provides a pulse when an error is detected. Useful for triggering an alarm while doing long-term monitoring.

Minimum pulse width	128 clock periods
Transition time	<500 ps
Output levels	1000 mV nominal (0 V to 1 V low-high)
Interface	SMA female

Trigger output

Provides a pulse trigger to external test equipment. It has two modes:

Divided Clock Mode: Pulses at 1/256th of the clock rate

Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns).

Minimum pulse width	128 clock periods (Mode 1) 512 clock periods (Mode 2)
Transition time	<500 ps

Trigger output

Transition time	>300 mV amplitude, 650 mV offset
Interface	50 Ω SMA female

Error detector rear panel connections

Detector start input

Used to trigger the acquisition of incoming data into the Error Detector reference pattern memory. High level starts capture.

Amplitude	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 serial clock periods
Maximum repetition rate	512 serial clock periods
Interface	SMA female, >1 kΩ impedance into 0 V

Error correlation marker input

Allows an external signal to provide a time-tagged marker to be placed in the error data set.

Logic family	LVTTL (<0.5 V Low, >2.5 V High)
Threshold	+1.2 V
Minimum pulse width	128 clock periods
Maximum repetition rate	512 serial clock periods
Maximum frequency	<4000 markers/s recommended
Interface	SMA female, >1 kΩ impedance into 0 V

General specifications

All specifications are guaranteed unless noted otherwise. All specifications apply to all models unless noted otherwise.

PC-related specifications

Display	TFT touch screen 640×480 VGA
Touch sensor	Analog resistive
Processor	Core2Duo or better
Hard disk drive	128 GB or greater
DRAM	2 GB or greater
Operating system	Microsoft Windows 7 Professional
Remote control interface	IEEE-488 (GPIB) or TCP/IP
Supported interfaces	VGA display USB 2.0 (6 total, 2 front, 4 rear) 100BASE-T Ethernet LAN IEEE-488 (GPIB) Serial RS-232

Physical characteristics

Height	220 mm (8.75 in.)
Width	394 mm (15.5 in.)
Depth	520 mm (20.375 in.)
Weight	
Instrument only	25 kg (55 lb.)
Shipping	34.5 kg (76 lb.)
Power	460 W
Voltage	100 to 240 VAC (±10%), 50 to 60 Hz

Environment characteristics

Warm-up time	20 minutes
Operating temperature range	10 °C to 35 °C (50 °F to 95 °F)
Operating humidity	Noncondensing at 35 °C (95 °F), 15 to 65%
Certifications	LVD Low Voltage Directive, US Listed UL61010-1, Canada Certified CAN/CSA 61010-1

Ordering information

BERTScope BSX series models

All Models Include: user manual, power cord, mouse, three (3) short low-loss cables

BSX125	BERTScope BSX-series 12.5 Gb/s Bit Error Rate Analyzer
BSX240	BERTScope BSX-series 24 Gb/s Bit Error Rate Analyzer
BSX320	BERTScope BSX-series 32 Gb/s Bit Error Rate Analyzer
BSXCV125	Conversion of BSA-C series BERTScope instruments to a 12.5 Gb/s, BSX125
BSXCV240	Conversion of BSA C-series BERTScope instruments to a 24 Gb/s, BSX240
BSXCV320	Conversion of BSA C-series BERTScope instruments to a 32 Gb/s, BSX320

Clock recovery instruments

CR125A	12.5 Gb/s Clock Recovery Instrument
CR175A	17.5 Gb/s Clock Recovery Instrument
CR286A	28.6 Gb/s Clock Recovery Instrument

BSX options

Opt. FEC	Forward error correction emulation
Opt. UPM	User-defined detector pattern match
Opt. F2	F/2 jitter generation
Opt. J-MAP	Add jitter decomposition software
Opt. LDA	Add live data analysis software
Opt. STR	Stressed signal generation
Opt. SLD	Add stressed live data option software
Opt. TXEQ	Add 4-tap Tx equalization
Opt. C3	Calibration Service 3 Years
Opt. R3	Repair Service 3 Years (including warranty)
Opt. R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of customer instrument purchase

Recommended accessories

BSXSICOMB	Sinusoidal interference combiner kit
BSXPCI3EQ	Eye opener kit for PCIe Gen3
BSXPCI4EQ	Eye opener kit for PCIe Gen4
LE160/LE320	16 Gbps / 32 Gbps, 2-channel linear equalizers
CR125ACBL	High-performance Delay Matched Cable Set (required for BERTScope and CRU in SSC applications)
100PSRTFILTER	100 ps Rise Time Filter
BSA12500ISI	Differential ISI Board
PMCABLE1M	Precision Phase Matched Cable Pair, 1 m
BSARACK	BSA/BSX-Rackmount Kit

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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