BERTScope™

BERTScope CR
Clock Recovery Instrument

- Instrumentation quality clock recovery
- 150 Mb/s–12.5 Gb/s continuous data rate coverage
- Accurate variable loop bandwidth from 100 kHz to 12 MHz
- Auto lock capability with LED display
- Programmable peaking adjustment with first and second order rolloff capability
- Self-measured and displayed PLL frequency response
- USB control connection to BERTScope or stand alone operation via front panel
- Single-ended or differential 50 Ω inputs/outputs
- DC coupled data through path data
- Full and divided clock outputs with selectable divide ratios
- Measurement of clock phase deviation as a function of frequency and time
- Data measurement capability
  - Edge Density Measurement —determine the mark density of the signal under test
- Ideal for spread spectrum clock (SSC) applications with large frequency excursions

SYNTHESYS
RESEARCH, INC.

The Vision of a Scope, the Confidence of a BERT,
And Clock Recovery you can Count on.

Compliant Clock Recovery

Many communication standards now specify that jitter testing must be carried out using a reference clock that has been derived from the data signal. Typical phase lock loop (PLL) characteristics are specified in terms of the -3 dB bandwidth of the recovery loop, the rate of rolloff of the frequency response, and the degree of response peaking allowable.

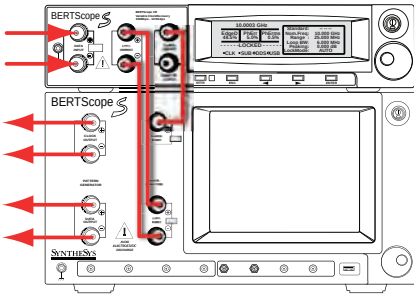
The BERTScope CR's advanced architecture measures and displays the PLL frequency response from 100 kHz to 12 MHz; the highest loop bandwidth available for jitter testing on the market today. The first clock recovery instruments to allow full control of parameters including loop bandwidth, peaking/damping and rolloff.

Design and test engineers can now find and lock onto signals of undefined or unknown data rate. The engineer can recover full rate clocks, including spread spectrum clocks, for signals at data rates from 150 Mb/s to 12.5 Gb/s. The engineer has full control of key parameters for variable loop bandwidth, peaking/damping and first and second order rolloffs, optimizing jitter tracking.

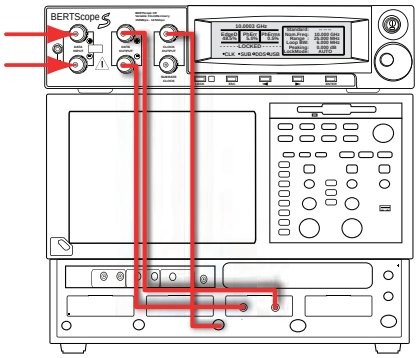
GOLDEN PLL

Many test standards require the use of a Golden PLL (phase lock loop.) Control of the BERTScope CR variable loop bandwidth allows for control of the jitter transferred to the recovered clock. When the loop bandwidth setting is narrow, much of the high frequency jitter is removed from the clock signal. The narrowest LBW setting is desirable when a clock with the lowest possible jitter is required. When the loop bandwidth setting is wide, jitter is transferred to the recovered clock, emulating a clock signal similar to the CDR of the receiver under test. Each standard provides an optimum LBW setting for clock recovery often called the Golden PLL.

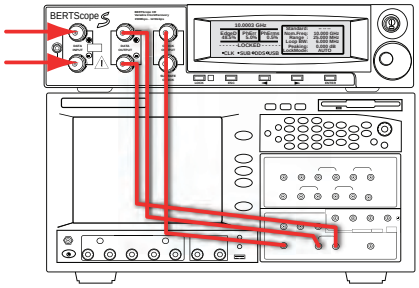
BERTScope CR Can Be Used with Any Sampling Oscilloscope, BERT or Pattern Generator



Connecting the BERTScope CR clock recovery instrument to the BERTScope Analyzer



Connecting the BERTScope CR clock recovery instrument to a sampling oscilloscope

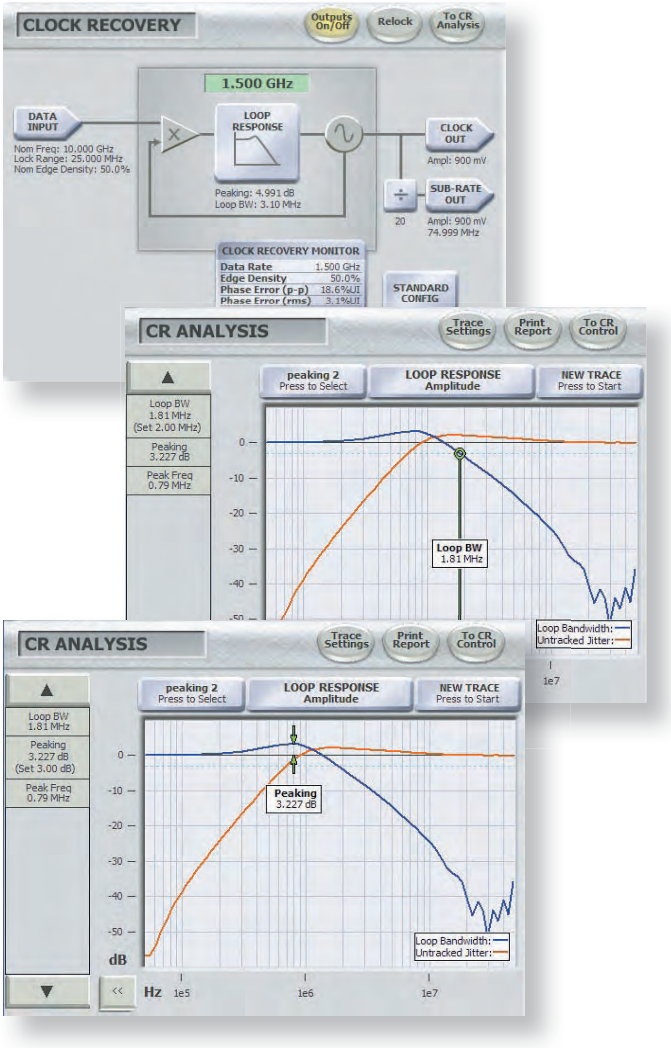


Connecting the BERTScope CR clock recovery instrument to a BERT

BERTScope CR Works Seamlessly with BERTScope Signal Integrity Analyzer

You can utilize the clock recovery instrument with the BERTScope Analyzer by connecting the USB cable between the two instruments.

The graphing capability can be displayed on the BERTScope Analyzer by pressing the “To CR analysis” soft key.



Recover Clocks for Optical Storage, Enterprise and Telecom Testing

The BERTScope CR has been designed from the ground up to provide users with flexibility and accuracy in compliance measurements. The HS model utilizes high sensitivity data inputs (40 mV single ended, 20 mV differential) with buffered data outputs. It is ideal for optical test applications, like 4X/8X Fibre Channel and 10G Ethernet standards, where the signal under test must be split off and converted from optical to electrical before being fed into the clock recovery data input. The BERTScope CR recover a full-rate clock up to 12.5 Gb/s, an important requirement for testing XFP and other 10 Gb/s MSA modules. The BERTScope CR is also the model of choice in electrical applications where the additional data input sensitivity is critical to the test setup.

Connecting the BERTScope CR to the Picometrix Reference Receiver

The Picometrix receiver should be used with a DC block. For DC coupling, the reference receiver requires +3V termination.

10 Gb/s Optical Reference Receiver with Wide Wavelength Coverage from 700–1650 nm.

Model AD-50xr/RR

Picosecond Pulse Labs DC Block
Bandwidth 7 kHz to >26 GHz
10 ps Risetime
Clean Transient Pulse Response

Model 5501A-121

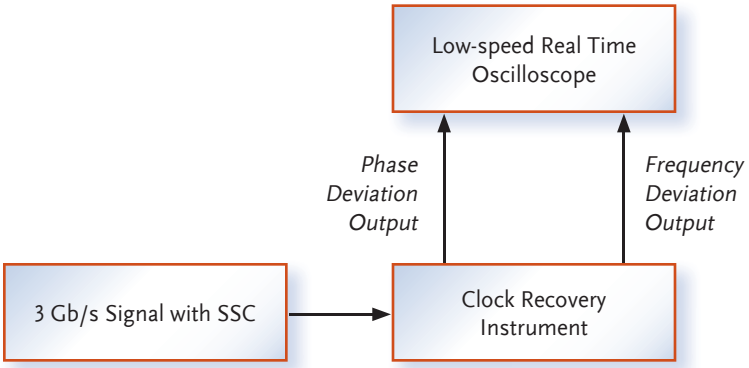
Recover Spread Spectrum Clocks for Testing to Electrical Serial Bus Standards

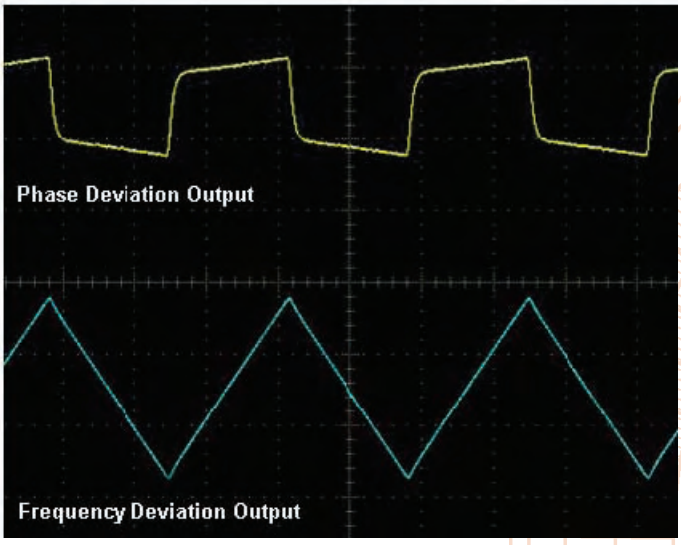
Spread Spectrum Clocking (SSC) is an increasingly required feature of serial bus standards. When employed, it can prove difficult to track but its effect must be included in test. These instruments are able to track SSC correctly with large frequency excursions up to 5000 ppm, making them unique amongst clock recovery test solutions. The BERTScope CR is the first clock recovery instrument to recover clocks from spread spectrum clocked signals used in Serial ATA, SAS, PCI Express and FB DIMM applications.

Spread spectrum clocks exhibit low frequency (30-33 kHz) modulation, for example, resulting in 225 UI deviation when imposed on a 3 Gb/s data signal. This frequency deviation is tracked accurately by the clock recovery instrument when the optional 5 piece cable set is used with the BERTScope CR and BERTScope Analyzer. This cable set is matched to compensate for the 5ns delay in BERTScope Analyzer with SSC signals, thus avoiding jitter amplification.

A signal with SSC was measured with the BERTScope CR. Outputs on the rear panel of the instrument provide monitoring points to view the loop behavior. When viewed on a low-bandwidth, real-time oscilloscope, the triangular waveform characteristic of SSC is visible in the lower trace. The upper waveform displays the difference in phase between data input and clock recovery output.

Optional 5-piece cable set





User Interface

The instruments can be used with the BERTScope Stress Analyzer AND in stand-alone operation. Inexperienced users and experts alike will respond to the same ease and accuracy already available in the BERTScope S Signal Integrity Analyzer. Perfect companions to the BERTScope, the clock recovery instruments smoothly integrate with the analyzer, seamlessly sharing a common user interface. A single USB connection and supplied high-quality microwave coax cables connect the two units together—that is all that is required to start measurements. The BERTScope automatically senses the presence of the Clock Recovery instrument, and control is achieved through the Clock Recovery setup screen. It's that simple. Additional information is also immediately available on the front panel display, showing parameters such as the PLL bandwidth, lock status, bit rate, peaking and rolloff. The system is designed to make sure that you are always aware of the test conditions, always aware of the factors in play that will affect your measurement results.

Graphing capability on the BERTScope analyzer allows users to plot loop response and inverse response curves for the settings in use, the -3 dB point and peaking values are also measured and clearly displayed.

For engineers wanting to utilize test equipment already available on their lab bench, the BERTScope CR is controllable via the front panel for stand alone operation. In keeping with the BERTScope family's philosophy of being the easiest to use signal integrity

An instrument front panel display gives critical information on the measurement being made, and settings can also be managed through the knob and 4 buttons located below the display, along with a lock button and LED indicator. This combination ensures that you are never lost, always certain whether the measurement you are making includes the effects of clock recovery.

The data outputs give the passed-through data signal. The output connectors provide a buffered version of the data input.

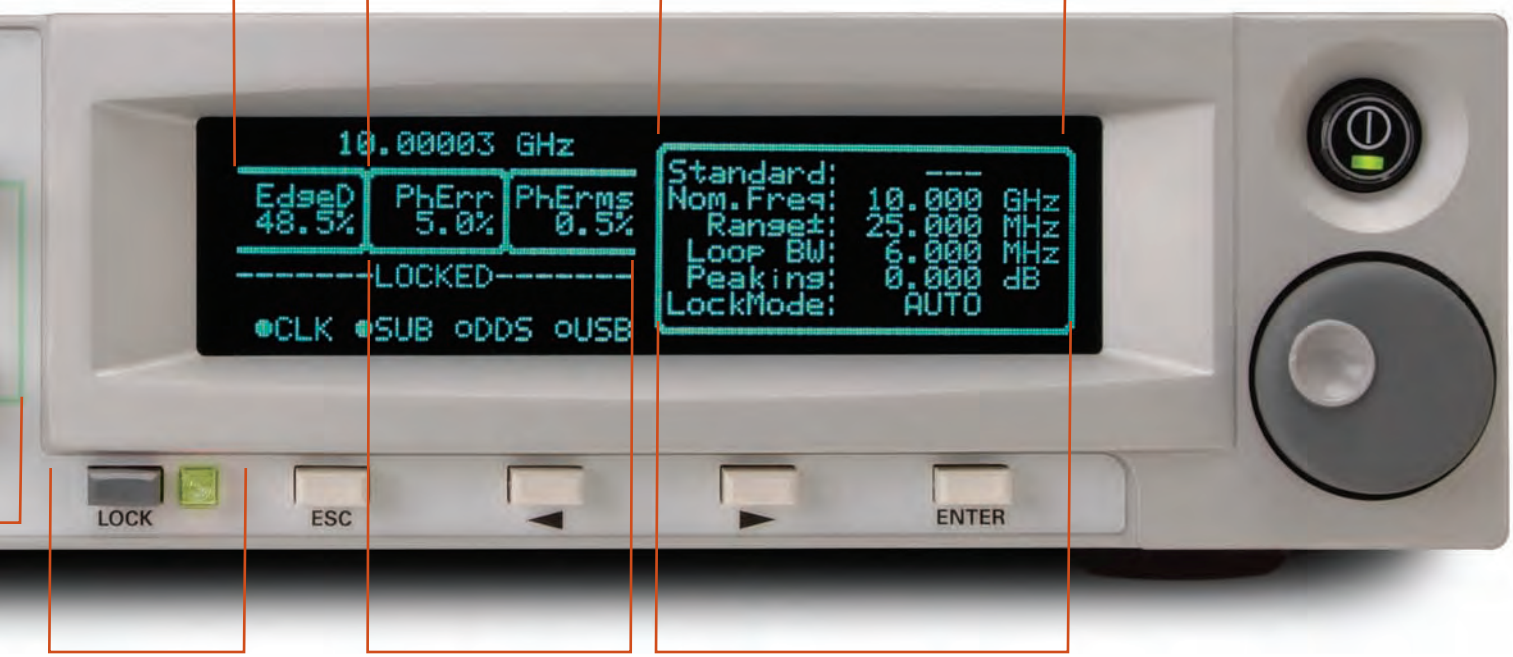
- **Clock Out and Sub-rate Clock Out** The clock recovery instrument offers full rate clock out to 12.5 Gb/s and sub-rate clock out at all the popular divide ratios (see listing on page 10.)

tools available, the clock recovery instrument provides the information you most need, right up front. For easy verification of compliance, the correct characteristics are automatically set when a given standard is selected from a pull-down menu. However, for users wanting to explore the limits of their designs, full control of parameters is also easily available. A good example of this is for systems where restricting the build-up of jitter is critical. Clock recovery plays a crucial role in this, and the ability to emulate a clock recovery source with excessive peaking is a great way of understanding the system sensitivity to jitter gain. The CR has variable jitter peaking that goes way beyond simple compliance, and allows jitter gain in excess of 10 dB if desired.

Remote control of the instrument is easily accessible via USB through BERTScope S analyzer. TCP/IP and GP-IB protocol interfaces are supported via USB and software developers kit.

- **Edge Density** The user has the ability to adjust the desired LBW to the edge density of the signal under test. The edge density is monitored and then optimized through loop gain settings. The clock recovery locks on data patterns with 10% to 100% edge densities.

- **Device Settings** nominal frequency of the data input signal, loop bandwidth, and peaking (up to 6 dB) are configurable on the front panel display.

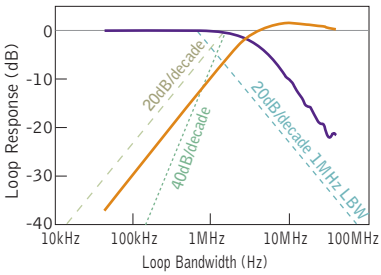


- **Lock modes** Manual and auto modes are supported. Locking status is displayed as locked—LED green, locking—LED amber, unable to lock—LED red. Lock range, min 10 MHz, max 500 MHz

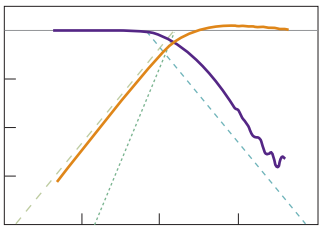
- **Phase Deviation** The clock extraction circuit produces a phase difference between incoming data and CR clock output. The phase deviation is displayed in % peak-peak and % RMS, with 10% min–90% max available range.

- **Standards** 24 industry standards have been pre-programmed into the clock recovery firmware, available via the front panel interface. Custom settings can also be programmed and saved for future use.

Standards Coverage

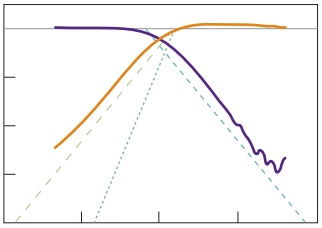


10 Gigabit Ethernet
Bit Rate: 10.3125 Gb/s
Loop Bandwidth: 4 MHz
Peaking: 0 dB

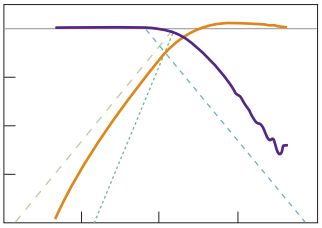


XAUI
Bit Rate: 3.125 Gb/s
Loop Bandwidth: 1.875 MHz
Peaking: 0 dB

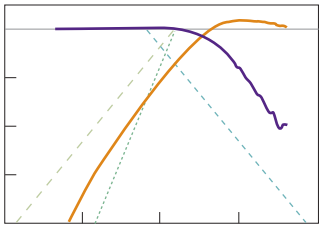
The small graphics show compliance settings, and the accompanying table shows common standards, the data rates they employ, and the loop bandwidths required for compliance measurements. The clock recovery instruments encompass a class-leading majority of the common standards, including those listed in the table. This ensures that your current and future needs will be covered for compliance and beyond.



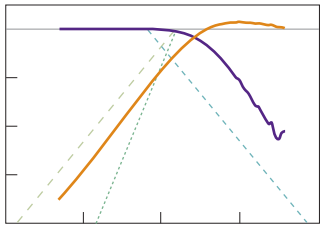
2x Fibre Channel
Bit Rate: 2.12 Gb/s
Loop Bandwidth: 1.275 MHz
Peaking: 0.3 dB max



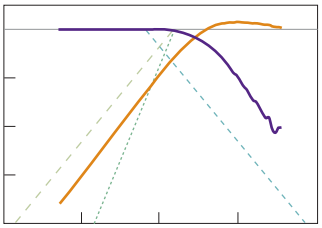
4x Fibre Channel
Bit Rate: 4.25 Gb/s
Loop Bandwidth: 2.55 MHz
Peaking: 0.3 dB max



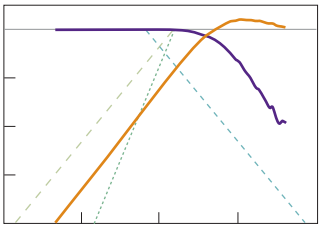
8x Fibre Channel
Bit Rate: 8.5 Gb/s
Loop Bandwidth: 5.1 MHz
Peaking: 0.3 dB max



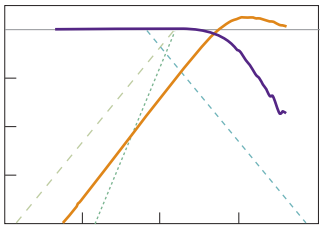
OIF CEI 6G+
Bit Rate: 6.25 Gb/s
Loop Bandwidth: 3.6 MHz
Peaking: 0.1 dB max



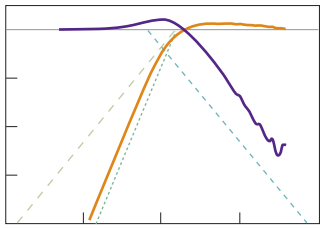
OIF CEI 11G+
Bit Rate: 11.0 Gb/s
Loop Bandwidth: 4 MHz
Peaking: 0.1 dB max



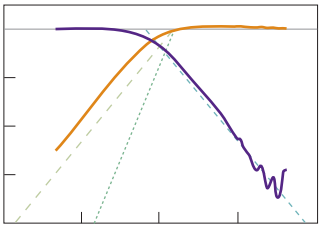
OIF CEI 11G+
Bit Rate: 11.0 Gb/s
Loop Bandwidth: 6 MHz
Peaking: 0.1 dB max



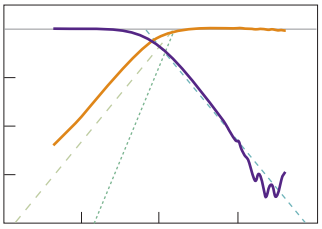
OIF CEI 11G+
Bit Rate: 11.0 Gb/s
Loop Bandwidth: 8 MHz
Peaking: 0.1 dB max



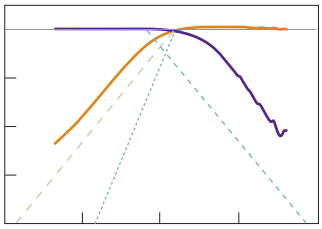
Serial ATA Gen 2, $f_{baud}/500$
Bit Rate: 3.0 Gb/s
Loop Bandwidth: 6 MHz
Peaking: 2.1 dB



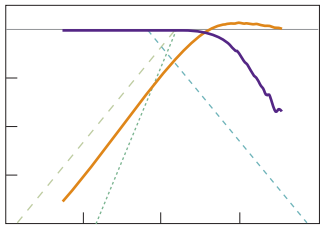
Serial ATA Gen 1, $f_{baud}/1667$
Bit Rate: 3.0 Gb/s
Loop Bandwidth: 0.9 MHz
Peaking: 0 dB



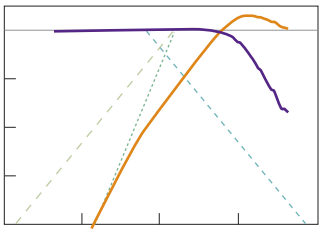
SONET OC-48/ SDH STM-16
Bit Rate: 2.488 Gb/s
Loop Bandwidth: 1 MHz
Peaking: 0 dB



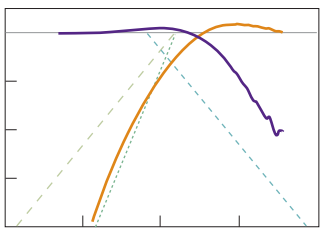
SONET OC-192/ SDH STM-64
Bit Rate: 9.95 Gb/s
Loop Bandwidth: 4 MHz
Peaking: 0 dB



XFP/XFI
Bit Rate: 10. 5 Gb/s
Loop Bandwidth: 8 MHz
Peaking: 0.1 dB max



Fully Buffered DIMM II
Bit Rate: 6.4 Gb/s
Loop Bandwidth: 11 MHz
Peaking: 0.5 dB



PCI Express II
Bit Rate: 5.0 Gb/s
Loop Bandwidth: 5 MHz
Peaking: 1 dB

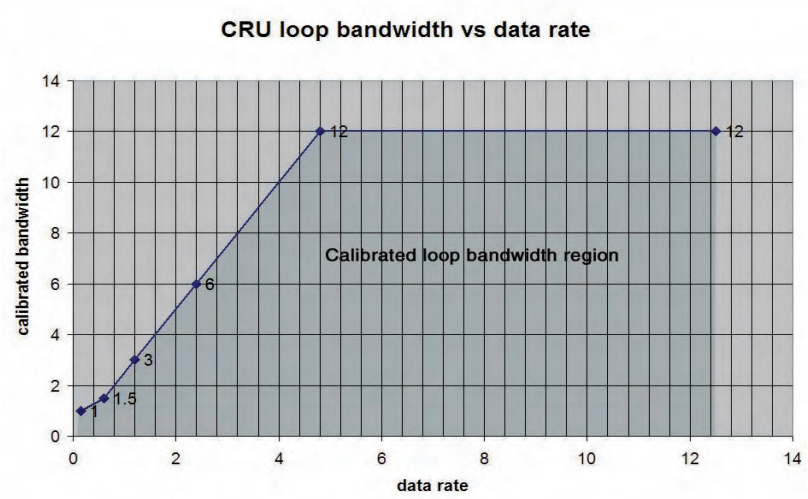
Notes:
1. Ripple at high loop bandwidths in these graphs is a feature of the measurement system rather than the loop.
2. The reference (dotted) lines are placed in identical positions in each graph to aid comparison.

Standard			Data Rate (Gb/s)	Common Clock Divide Ratios	Loop Bandwidth (MHz)	Peaking (dB)	Slope	Spread Spectrum Clocking	Notes
Ethernet	1.0				.637				
	10 Gb/s Ethernet Transmitter Test		10.312		≤4		-20 dB/ decade	No	
	XAUI		3.125		1.875				
Fibre Channel	1x		1.063	10	0.638	0.3 max	-20 dB/ decade	No	
	2x		2.12	20	1.275	0.3 max			
	4x		4.25	40	2.550	0.3 max			
	8x		8.5	80	5.100	0.3 max			
OIF CEI	6+ Gb/s		4.976 to 6.375		3.6 (f_{baud}/1667)	0.1 max	-20 dB/ decade	No	8 MHz for most tests for ITU applications, BW/1667 other. Minimum of 4 MHz for stress testing in one case.
	11+ Gb/s		9.95 to 11.1		8, ITU 6 (f_{baud}/1667) other				
SATA (See note +)	Gen 1	250UI	1.5	15	6.000			Yes	Gen 1 & 2 categories: 'i' (internal, hard drives etc.) and 'm' (medium reach) use f_{baud}/500 and f_{baud}/10 for Gen 2 and 250UI and 5UI for Gen 1. 'x' (extended reach) uses f_{baud}/1667, Type 2. This is same as SAS. * Implied: spec'd as damping factor of 0.707 min to 1.00 max– conversion taken from Gardner. + Loops bandwidths spec'd with transition density of 1 (100% or 1010101 pattern). Assumption is that loop bandwidth will change proportionally as transition density reduces.
		f_{baud}/1667			0.900	2.09 - 1.25 dB*	Type 2		
		5UI			300.000				
	Gen 2	f_{baud}/500	3	30	6.000	2.09 - 1.25 dB*	Type 2		
		f_{baud}/1667			1.800	2.09 - 1.25 dB*	Type 2		
		f_{baud}/10			300.000	2.09 - 1.25 dB*	Type 2		
SONET/ SDH	OC12/STM-4		0.622		0.250		-20 dB/ decade	No	
	OC48/STM16		2.488		1.000				
	OC192/STM-64		9.95		4.000				
XFP/XFI	XFP/XFI	Receiver Test	9.95–11.2	64	8.000	0.1 max		No	
		Transmitter Test			4.000	0.1 max	-20 dB/ decade		
Fully Buffered DIMM	FB-DIMM1		3.2, 4.0	24	11 to 33	0.5 to 3	2nd Order	Yes. — Transmitter Test: Full SSC swing — Receiver Test: 0.06 UI swing	
			4.8	24	11 to 22				
	FB-DIMM2		4.8, 6.4, 8.0, 9.6	Forwarded Clock	11 to 22	0.5 to 2			
PCI Express	I		2.5	25	1.500		1st order with -20 dB/ decade	Yes, Optional. — Receiver Test: 65 ps pk-pk swing	
	II		5	50	5 to 16 8 to 16	Up to 1 dB Up to 3 dB	1st or 2nd order		
SAS	Gen 1	f_{baud}/1667	1.5	15	0.900		1st order (single pole)		* Implied: spec'd as damping factor of 0.707 min to 1.00 max– conversion taken from Gardner. + Loops bandwidths spec'd with transition density of 1 (100% or 1010101 pattern). Effective loop bandwidth will change proportionally as transition density reduces.
	Gen 2	f_{baud}/1667	3	30	1.800		1st order (single pole)		

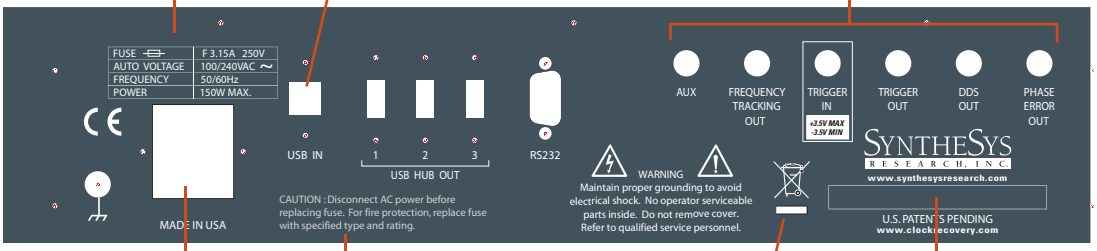
Instrument Specifications

Data Inputs/Outputs	
Data Interfaces	50Ω differential or single-ended, DC-Coupled. APC 3.5 User-Replaceable Planar Crown® adapters
Data Rate Coverage	150 Mb/s to 12.5 Gb/s
Data Insertion Loss	2 dB (min), 2.6 dB (typical), 3 dB (max) from data input to data output
Data Input Voltage Range	-5 V (min), +5 V (max)
Input Sensitivity	100 mV single ended (typical) 50 mV differential (typical)
Measured Edge Density	± 1%
Measured phase deviation	Displayed as % RMS and % peak-peak, 10%–90% peak-peak available range
Buffered Data Outputs	
Output Amplitude	Not applicable
Clock Outputs	
Clock Interfaces	50Ω single-ended, AC Coupled. APC 3.5 user-replaceable Planar Crown® adapter
Clock Output Range	150 MHz to 12.5 GHz (Full Rate Clock Output)
Loop Bandwidth	100 kHz–12 MHz variable.
Loop Bandwidth Accuracy	± 5%
Locking Range	50 MHz default, adjustable to 10–500 MHz
Peaking	0–6 dB from 500 kHz to 12 MHz, 0 dB from 100 kHz to 500 kHz
Peaking accuracy	Greater of ±10% of setting, or 0.2 dB
Frequency Response	-20 dB/decade to -40 dB/decade
Intrinsic Jitter (Typical)	70 fs (typical), 250 fs RMS (max), measured at 800 mV peak-peak input amplitude, 10 Gb/s, 1010 pattern, 2 MHz loop bandwidth setting and 0.5 dB peaking
Output Frequency Deviation Tracking Range (Tracking 30 to 33 kHz Triangle Modulated SSC)	+500/-5500 ppm (+0.05/-0.55%)
Return Loss	15 dB
Output Waveform Rise/Fall Times (20/80%)	25 ps (typical), 30 ps (max)
Output Amplitude	250 mV (min), 1.5 V (max), 900 mV peak-peak (typical)
Output Amplitude Setting Accuracy	Greater of 10% or 30 mV
Sub-rate Clock Output *as specified for clock output except for the following:*	
Sub-rate Divider Ratios	Full rate divided by 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 49, 50, 54, 56, 60, 63, 64, 70, 72, 80, 81, 90, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648
Trigger Output *(Rear Panel)*	
Interface Type	SMA, 50Ω dc coupled
Latency	300 ms
Trigger Input *(Rear Panel)*	
Interface Type	SMA, 50Ω dc coupled to 0V
Threshold	1.5 V
Minimum Pulse Width	50 ns
Control	
Device Info	Serial number, revision codes available via front panel display
Control Interface	USB cable (supplied). Unit also provides hub capability giving 3 additional USB ports.
Physical and Environmental	
Dimensions	15.5" wide X 3.75" high X 13.25" deep
Weight	20 lbs
Temperature Operating Non-Operating	 0 to 40°C -18 to 60°C
Relative Humidity Operating Non-Operating	 20 to 80% at or below 40°C 5 to 90% at or below 60°C
Vibration (5 Hz to 500 Hz) Operating Non-Operating	 0.2 g RMS 2.09 g RMS

Clock Recovery Loop Bandwidth vs Data Rate



The BERTScope CR has a variable loop bandwidth from 100 kHz to 12 MHz. The *calibrated* loop bandwidth is limited by the graph at left.



The WEEE directive indicates the user must not discard this electronic product in domestic household waste. To dispose of this product, contact SyntheSys Research or see the website at www.bertscope.com for more information.

The BERTScope CR comes with USB cable, US power cord, optional clock and data cables for use with BERTScope analyzer, SMA terminations for data outputs, and quick start guide. A replacement fuse is also included.

BERTScope CR Specific Cautions

⚠	To prevent damage to the instrument when the data outputs are not in use, terminate the data outputs with the SMA terminations provided.
⚠	To prevent damage to the high sensitivity data circuitry, ensure that the input voltage does not exceed ± 5 V range, 3 V peak-peak.

Ordering information

Part Number	
CR 12500A	12.5 G Clock Recovery Instrument
CR 12500A BN	Bundle option when clock recovery purchased at the same time as a BERTScope instrument.
Options:	
CR 12500ACBL	High Performance Cables
	This option adds one set of 5 high performance cables for use with the BERTScope analyzer to compensate for CR clock to data delay and BERTScope analyzer clock to data delay. The Huber+Suhner high performance cables include phase matched pairs of data input (1 meter) and data output (2 meter) cables, and one 0.2 meter clock out cable.
CR 12500A3YR	Extended Warranty
	Extended warranty adds two year extension to the standard one year product warranty. All warranties include both hardware repair and software updates. System repair or replacement is at SyntheSys Research discretion. All repairs are returned to factory at Menlo Park facility. Warranty includes cost of ground freight for return shipment. Extended warranties must be ordered within one year of initial delivery.
CR 12500ACAL	CR 12500A Calibration
	Calibration of CR 12500A Clock Recovery Unit to original factory specifications. Any required repairs will be billed separately. Calibration certificate is included.

Related Product literature:

- BERTScope CR Quick Start Guide
- Posters
  Anatomy of Clock Recovery Part I
  Anatomy of Clock Recovery Part II

About BERTScope™

BERTScope™ is a trademark of SyntheSys Research, Inc., a privately held California corporation founded in 1989 with the mission to develop advanced test instruments for identifying and locating the source of errors in high-speed digital bit streams. BERTScope CR pairs with BERTScope to offer the vision of a scope, the confidence of a BERT, and clock recovery you can count on. More information is available at www.bertscope.com.

SYNTHESYS RESEARCH, INC.

3475-D Edison Way
Menlo Park, CA 94025 U.S.A.
Phone 650 364-1853
Fax 650 364-5716

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