Agilent U4301A

PCI Express® 3.0
Analyzer Module

Data Sheet

Agilent solutions for PCIe Gen1 to Gen3 analysis and emulation.

- PCI Express generation 1, 2, & 3 protocol architecture
- Lane speeds 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s
  - Lane widths x1, x4, x8, and x16
  - Stimulus response testing with the addition of the U4305A protocol exerciser
- NVMe device analysis and emulation
  - Compact AXIe modular system configuration

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OVERVIEW

Product description

Agilent Technologies' high speed U4301A PCI Express® 3.0 analyzer module is a protocol analyzer supporting all PCI Express® applications from Gen1 through Gen3 and speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3) and with link widths from x1 to x16. The U4301A analyzer captures and decodes PCI Express data and displays it in a packet viewer window.

The U4301A analyzer is a blade that is installed in an AXIe two slot M9502A or five slot M9505A.

Probing is provided by the U4321A solid slot interposer probe, U4324A flying lead solder down probe, or the U4322A mid bus probe based on Agilent's equalization snoop probe (ESP) technology.

Stimulus and response testing of the PCIe system is accomplished with the addition of the U4305A PCIe Gen3 exerciser.

A link training status state machine (LTSSM) exerciser provides stimulus for testing PCIe links up to the full speed of Gen3 systems. The analyzer LTSSM overview can pinpoint specific training sequence issues through easy to interpret analysis results.

Agilent's Transactional decoder includes a transactional viewer that allows the designer to select transactional queues and performance information from the analyzer's NVMe transaction overview pane. This organizes the transactions by direction or by queue to follow the data flow across the interface, with one-click control. Individual PRP (Physical Region Page) lists contain all of the key information of the NVMe queues, allowing designers to quickly review and validate the data flows over the PCIe connections.

The Performance analysis package includes the real data throughput calculations, with response-time measurement of the PCIe data flow. It allows designers to measure and understand throughput performance, PCIe response times, and other operational measurements that provide the insight needed to optimize device performance.

Analysis and debug

- Support for Gen1 through Gen3, x1 through x16 link width
- 4 GB of capture buffer per module
- Non-intrusive probing that leverages ESP technology

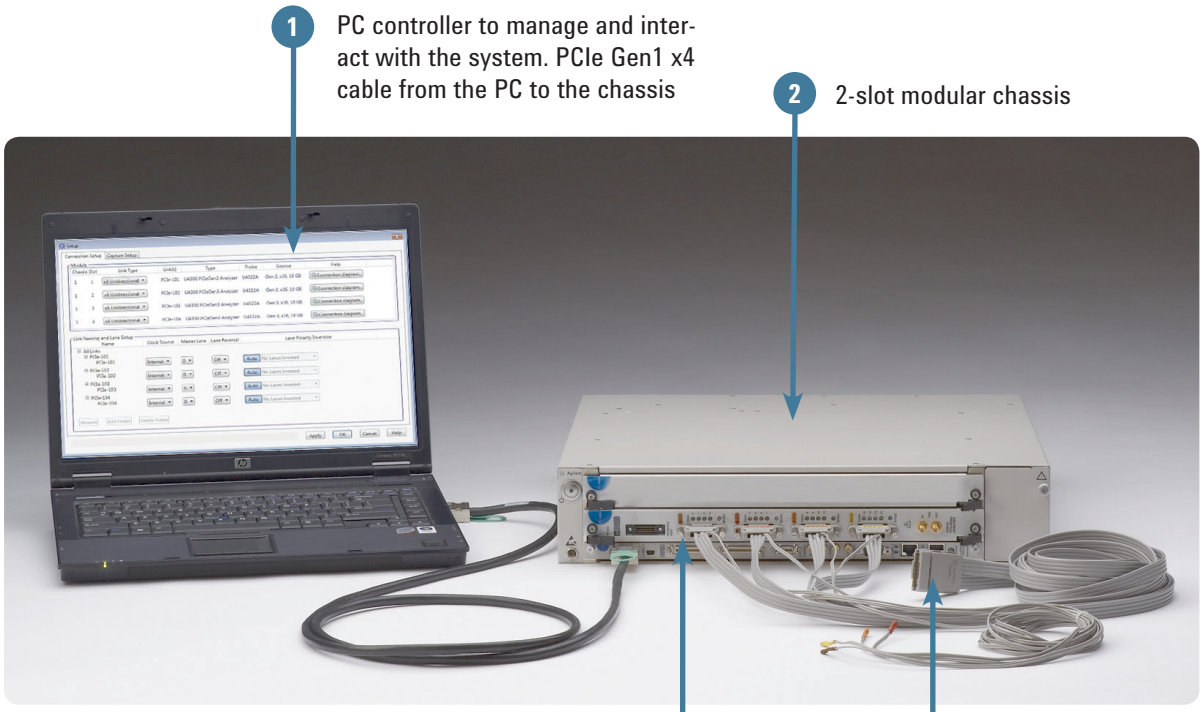
Industry leading probes

- The mid-bus probe supports x1 to x16 unidirectional or x1 to x8 bidirectional
- The solid slot interposer will support x1 to x16 unidirectional or bidirectional
- The flying lead solder down probe offers support for x1 & x2 bidirectional capability on a single probe. Other standard lane width configuration support is x4, x8, & x16

Stimulus and test U4305A exerciser

- Support for Gen1 through Gen3 and link widths of x1 through x16
- Link testing from x1 through x16, using automated LTSSM exerciser
- PCIe, MR-IOV, and SR-IOV stimulus response testing
- INVMe Root Complex emulation for test and verification of NVMe devices
- Protocol test card (PTC) to measure PCIe Gen3 DUT port and system BIOS specification compliance as defined by the PCI SIG standards

SYSTEM ARCHITECTURE OVERVIEW



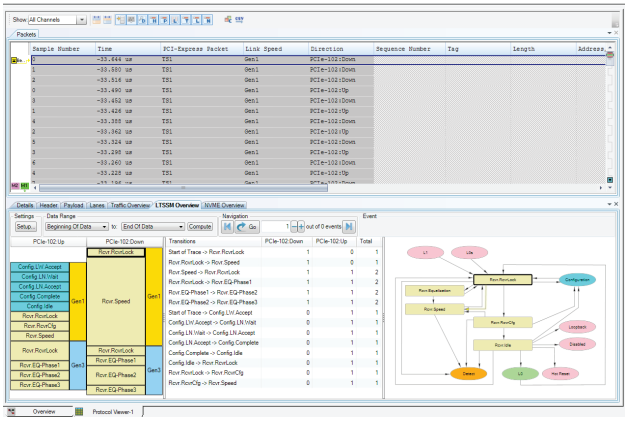
Configuration	
Step 1	Order the U4301A analyzer module Select the option for the number of lanes to be tested and software license for 5 Gbps or 8 Gbps applications Refer to ordering information for details
Step 2	Order a modular chassis Recommended chassis is the Agilent M9502A 2-slot AXIe chassis or optionally the Agilent M9505A 5-slot AXIe chassis
Step 3	Select a PC controller—Agilent recommends the M9536A embedded controller—or select an external PC that meets the performance requirements as specified in the *PXI and AXIe Modular Instrumentation,* Tested Computer List Technical Note (http://cp.literature.agilent.com/litweb/pdf/5990-7632EN.pdf).
Step 4	Order the probe for your measurement application • U4321A solid slot interposer 3.0: Order the option for the number of lanes to be tested • U4322A mid bus probe based on Agilent soft touch technology • U4324A flying lead solder down probe: Order the option for the number of lanes to be tested
Step 5	Add the exerciser for stimulus/response testing • U4305 exerciser: Order the option for the number of lanes to be tested and software licenses for number of lanes to be tested as well as applications such as end node or root complex emulation, LTSSM. MR-IOV, or SR-IOV emulation

1. *Note: The slot interposer and exerciser lane width is fixed and is not upgradable due to the connector size being a function of lane width. A smaller lane width probe can be used in a wider lane application, but only those lower lanes will be tested. Agilent does not recommend or support the use of lane converters.*

U4301A analyzer module

Effective presentation of protocol interactions from physical layer to transaction layer

- LTSSM Overview with full state transaction traffic capture at the PHY layer logic sub block
- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction
  - Easy flow columns to better understand the stimulus and response nature of the protocols
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for link training debug, config accesses and general I/O

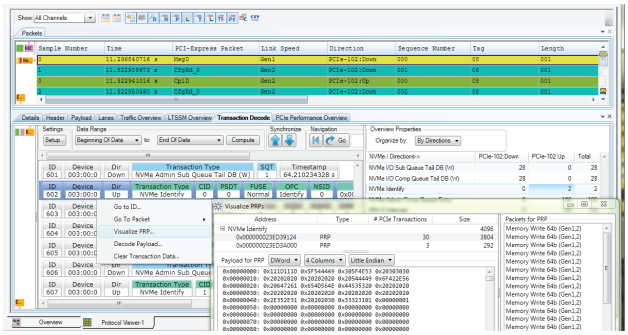


LTSSM analysis is easy with detailed tracking of each state transition and that is displayed in a linear state-view, state transition table and state bubble chart.

Transaction decode

The Transaction Decode tab in the Protocol Viewer window allows you to compute and view transactions decoded from the captured PCIe traffic. The decoding and display of transactions is done as per the relevant storage protocol specifications such as NVMe to help you easily correlate the decoded data to the protocol specifications and evaluate DUT's compliance to these specifications.

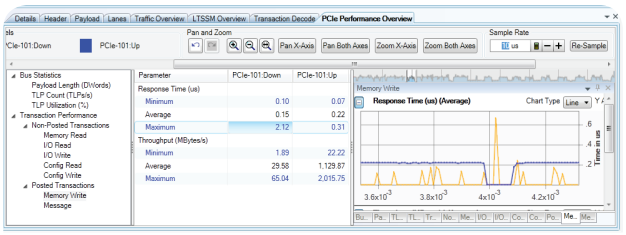
Transaction decoding of NVMe data includes analysis of the trace to identify all of the relevant transactions types to present a transaction overview table that enable quick and easy navigation of key packet types.



NVMe transaction information provides easy to understand displays of NVMe payloads and PRP messages. Transaction overview of all transactions enables instant access to all messages in the capture trace.

Performance analysis

The PCIe Performance Overview tab in the Protocol Viewer window allows you to perform post processing on the captured PCIe traffic to generate an offline performance summary of a wide variety of bus traffic including bus utilization and data throughput as well as transaction measures like response times and latency. These performance measures are displayed in tabular as well as charts form.

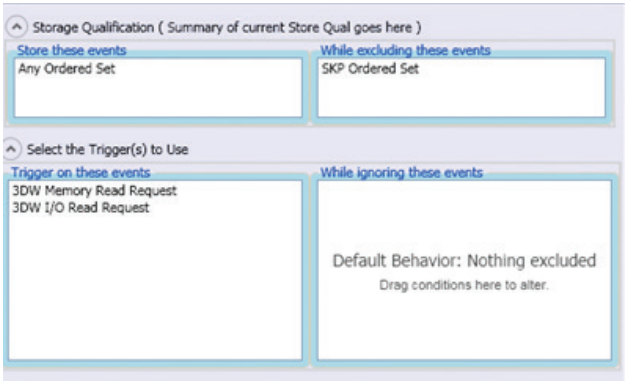


PCIe performance is calculated on bus utilization, throughput, and response times. These views provide the detail needed to calculate the operation performance of any device.

U4301A analyzer module *(Continued)*

Simple and powerful state-based triggering

- New simple trigger mode makes it easy to setup single event triggers
- Powerful state-based triggering including
  - Four states supported in trigger sequencer
  - Triggering on patterns (ordered set patterns or packet types)
  - Internal counters and timers
- External trigger in/out



Powerful hardware features ensure capture of important transition events

- Large capture buffer, for long recording sessions with 4 GB per module (x1-x8 bidirectional) and 8 GB for x16 bidirectional
- PCIe Gen1 x4 link to the host PC, provides up to 10 Gb/s of data download saving valuable test time
- LEDs to show lane status and speed for fast understanding of current link status

U4301A analyzer module characteristics and specifications

- Environmental specifications as per the main frame except maximum operating temperature = 40 °C
- Trigger input: Input Z = 50 ohms, Vmax = 3.3 V
- Trigger output: 2.0 V
- Minimum trigger duration: 20 ns

Host PC requirements

Select a PC controller--Agilent is proud to recommend the M9536A embedded controller--or select an external PC that meets the following performance requirements. Agilent has pre-tested a number of external PCs as listed in the *PXI and AXIe Modular Instrumentation,* Tested Computer List Technical Note (http://cp.literature.agilent.com/litweb/pdf/5990-7632EN.pdf).

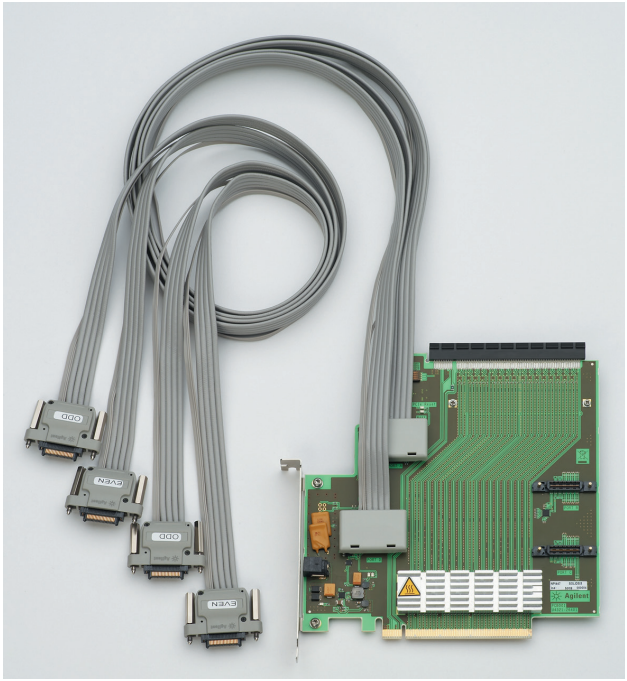
- Processor speed: 1 GHz 32-bit (x86) or 1 GHz 64-bit (x64) 2 GB minimum available memory running Windows XP Professional (32-bit) or Windows 7 (32-bit or 64-bit);
- Available hard disc space: 1.5 GB
- Support for DirectX 9 graphics with 128 MB graphics memory recommended, (Super VGA graphics is supported)
- Microsoft Internet Explorer 7 or greater
- Compatible with a PCIe Gen1 x4 interface module

Probing

Accurate data recovery with consistent representation of the signal

U4321A slot interposer

- ESP (equalizing snoop probe) technology ensures accurate data recovery in all Gen3 platforms and all link width x1 through x16
- High fidelity signal capture ensures design problems can be reproduced
- Mechanical stabilization for the device under test's (DUT's) end point and to ensure firm PCIe slot connections



Characteristics

- Power: 12 VDC, 1.25A max
- Power supply; Agilent part number 0950-5160
- Input: 100 to 250 VAC, 50 to 60 Hz

Accurate data recovery with flexible use model

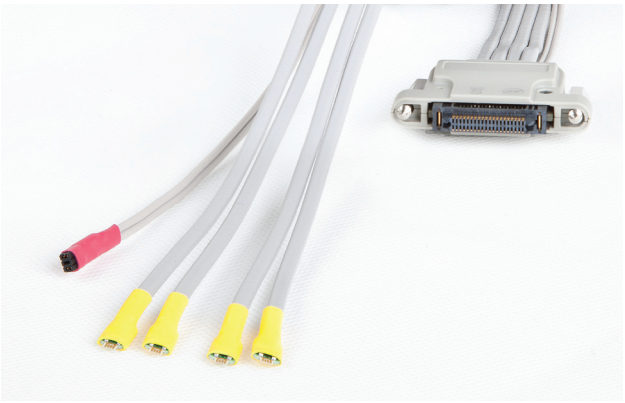
U4322A mid bus probe

- Provides signal capture in situations where no PCIe connector is available
- Micro spring-pin probe based on Agilent's soft touch technology provides reliable contact to signal pads
- Independent reference clock per four lanes for maximum layout flexibility

Characteristics

- Input: 25V max or 3 Vrms into 250 ohms
- Temperature: Operating 0 to 40 °C
- Storage –40 to 70 °C
- Humidity: 15 to 95% non-condensing
- Altitude: 3,000 m (10,000 ft)

Accurate data recovery with full channel mapping support & flexible probe points



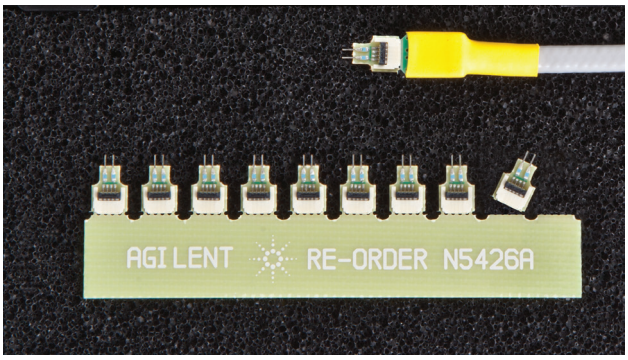
U4324A flying lead solder down probe

- Provides signal capture in situations where no PCIe slot connector or PCIe standard mid bus footprint is available.
- Low channel count per probe to reduce unnecessary expense for unused channel leads
- Independent reference clock tap for maximum layout flexibility
- Low cost, easily replaceable N5426A zero insertion force (ZIF) tips to maximize probe use life

Characteristics

- Input: 10 V max common mode
- Capacitive loading: 0.250 fF
- Temperature: Operating +5 to +40 °C
- Storage: –40 to 70 °C
- Humidity: Operating 80% RH @ 40 °C
- Storage: 90% RH @ 65 °C
- Vibration: 2.09 Grms (5 to 500 Hz random)
- Shock: 1.6 m/s [63 in/s] (2 mS half sine)

N5426A ZIF tip kit



- The ZIF tip is a connection accessory used to connect the U4324A flying lead cable to the channel on the DUT
- One side of the ZIF tip connects to the flying lead and is soldered to the DUT on the other end
- The ZIF tip is calibrated to the U4324A flying lead; no impedance changes should take place to the ZIF tip
- 10 ZIF tips per kit

Characteristics

- Input: 10 V max common mode
- Capacitive loading: 0.250 fF
- Temperature: Operating +5 to +40 °C
- Storage: –40 to 70 °C
- Humidity: Operating 80% RH @ 40 °C
- Storage: 90% RH @ 65 °C
- Vibration: 2.09 Grms (5 to 500 Hz random)
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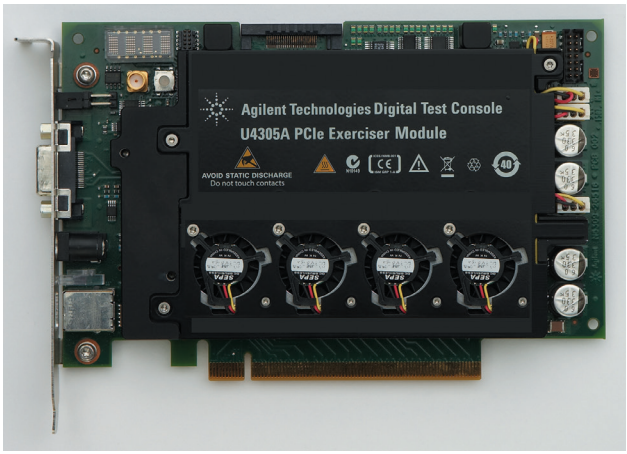
Thorough link testing U4305A PCI exerciser



- Addition of the U4305A provides PCIe,MR-IOV and SR-IOV stimulus response testing
- Predefined LTSSM sequences simplify state transition testing
- Predefined protocol test card (PTC) test cases applied to Lane 0 only, provide specification compliance feedback
- Full speed testing of Gen 1 through Gen 3 systems
- All lane widths supported at full speed
- End point emulation and act as a down stream component (DSC)
- Root complex emulation and act as an upstream component (USC)

Specifications

Refer to the U4305A data sheet pub number 5990-8458EN for detailed characteristics and specifications.

Related Agilent Literature

Publication title	Pub number
Hardware and Probing for PCI Express Gen3 User's Guide available at Agilent.com/find/U4301A	U4301-97000
PCIe 3.0 Analyzer User Guide	U4301-97001
PCI Express Design and Test – From Electrical to Protocol - Brochure	5989-5594EN
U4305A Protocol Exerciser for PCI Express® 3.0 - Data Sheet	5990-8458EN

ORDERING INFORMATION

U4301A analyzer module

A specific configuration is required to determine the lane width to be tested.

Model number	Description
U4301A-A01	Link width x1
U4301A-A04	Link width x4
U4301A-A08	Link width x8
U4301A-A16	Link width x16 *Note: Analyzing x16 requires the purchase of two U4301A-A16 modules.*
U4301A-AN2	Software license for PCIe Gen2, 5 Gbps
U4301A-AN3	Software license for PCIe Gen3, 8 Gbps
U4301A-1FP	LTSSM software license for fixed node, perpetual
U4301A-1NP	LTSSM software license for floating, server based
U4301A-2FP	Performance summary, software license for fixed node, perpetual
U4301A-2NP	Performance summary, software license for floating, server based
U4301A-3FP	Transaction Decoder, software license for fixed node, perpetual
U4301A-3NP	Transaction Decoder, software license for floating, server based

Modular chassis and computer interface

The recommended chassis is the 2 slot AXIe configuration.

Chassis type	Model number	PC configuration	Interface	Cable
AXIe (recommended)	M9502A 2 slot AXIe	Lap top	M9045A	Y1200A
		Desk top	M9047A	Y1200A

Probe selection

Probe type	Model number	Description
Solid slot interposer 8 Gbps ***Note:*** *The U4321A interposer probe lane width is fixed and is not upgradable to accommodate different lane widths due to the fact that the connector size is a function of lane width. Agilent does not recommend or support the use of lane converters.*	U4321A-A01	Link width x1
	U4321A-A04	Link width x4
	U4321A-A08	Link width x8
	U4321A-A16	Link width x16
Mid-bus probe	U4322A	Mid-bus probe based on Agilent soft touch technology for applications where no standard PCIe connector is available for testing
	U4322A-R05	Set of 5 retention modules
	U4317A	Gen3 to Gen2 mid bus adaptor
Flying lead probe	U4324A	4 channel/probe
	N5426A	ZIF tip kit (10 pcs)

ORDERING INFORMATION (CONTINUED)

Analyzer upgrades

Model number	Description
U4301U-2FP	Performance summary, software license for fixed node, perpetual
U4301U-2NP	Performance summary, software license for floating, server based
U4301U-3FP	Transaction Decoder, software license for fixed node, perpetual
U4301U-3NP	Transaction Decoder, software license for floating, server based
U4301U-AFP	Analyzer software license upgrade x1 to x4
U4301U-BFP	Analyzer software license upgrade x1 to x8
U4301U-CFP	Analyzer software license upgrade x1 to x16
U4301U-DFP	Analyzer software license upgrade x4 to x8
U4301U-EFP	Analyzer software license upgrade x4 to x16
U4301U-FFP	Analyzer software license upgrade x8 to x16

Stimulus/response tester

	Model number	Description
Exerciser card PCIe exerciser and PCIe LTSSM exerciser for PCIe 3.0, PCIe 2.0 and PCIe 1.0 ***Note:*** *The U4305A PCIe exerciser lane width is fixed and is not upgradable to accommodate different lane widths due to the fact that the connector size is a function of lane width. Agilent does not recommend or support the use of lane converters.*	U4305A-E01	Link width x1
	U4305A-E04	Link width x4
	U4305A-E08	Link width x8
	U4305A-E16	Link width x16
	U4305A-EX3	Software license for the exerciser
	U4305A-LT3	LTSSM software license
	U4305A-MR2	Multi-root visualization software license
	U4305A-1FP	NVMe RC exerciser, software license for fixed node, perpetual
	U4305A-1NP	NVMe RC exerciser, software license for floating, server based
	U4305A-022	ECRC testing
	U4305A- 023	SR-IOV emulation
	U4305A-024	Increase to 5 function emulation
PTC test suite for PCIe 3.0 and PCIe 2.0	U4305A-021	PCIe spec compliance test suite

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