

# Keysight Technologies

- N4877A Clock Data Recovery and Demultiplexer 1:2
- N1075A Optical Pick-Off/Converter
- N1070A Optical Clock Recovery Solution

## Version 1 Data Sheet



Electrical and Optical Clock Data Recovery Solutions up to 32 Gb/s

- Synchronization for receiver bit-error-ratio (BER) testing and transmitter waveform analysis
- Continuous tuning from 50 Mb/s to 32 Gb/s
- Ultra-low residual random jitter: < 100 fs RMS
- Optical and electrical configurations
- Golden phase-locked loop (PLL) operation with a tunable loop bandwidth from 15 kHz to 20 MHz for configurable industry-standard compliant test



## Electrical and optical clock data recovery solutions

Keysight Technologies, Inc. clock data recovery solutions offer an excellent data rate range from 50 Mb/s to 32 Gb/s making them ideal for many transmitter and receiver test setups for computer, datacom as well as communication standards.

The N4877A clock data recovery (CDR) and demultiplexer 1:2 is the core product of Keysight's CDR offering. Adjustable loop bandwidth and selectable peaking combined with high sensitivity and low intrinsic jitter performance, ensure accurate measurements. The built-in demultiplexer simplifies receiver testing with Keysight's BER testers (BERT) for data rates above 12.5 Gb/s.

The N1075A optical pick-off/converter provides an optical coupler that picks off optical energy to create an electrical signal for the N4877A CDR and demultiplexer. Together, the two instruments form the N1070A optical clock recovery solution. N1075A and N1070A are available as single-mode and multimode versions.

## PLL and jitter spectrum analysis

Use 86100DU-400 software to make fast, accurate and repeatable measurements of phase-locked loop (PLL) bandwidth/jitter transfer. A hardware clock data recovery like the N4877A, N1070A and 83496B can be configured as a jitter receiver which can be combined with a precision jitter source like the J-BERT N4903B to create a PLL stimulus-response test system. PCI Express® approved PLL bandwidth compliance tests and SONET/SDH jitter transfer measurements are preconfigured, with automatic report generation. The 86100DU-400 software also provide insights into the root causes of jitter through phase noise and jitter spectrum analysis on both clock and data signals.

## Keysight N4877A Clock Data Recovery and Demultiplexer 1:2



Figure 2. The N4877A recovers clock and demultiplex data from 50 Mb/s to 32 Gb/s

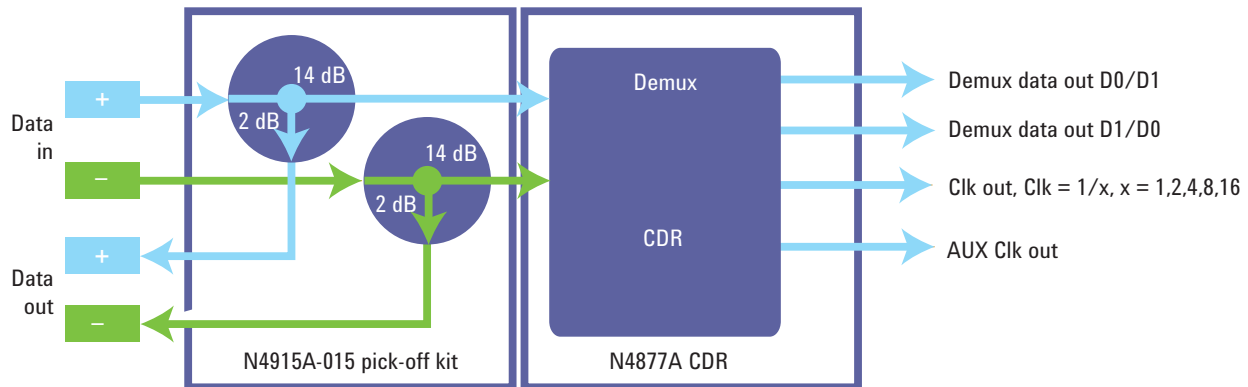


Figure 3. The N915A-015 pick-off kit is especially designed to be used with the N4877A and offers a bandwidth of 50 GHz. The demultiplexer data outputs can swap between even and odd bits.

### Accurate Clock Data Recovery and Demultiplexer for High-Speed Applications

- Recovers clock from data streams up to 32 Gb/s (Option 232)/16.5 Gb/s (Option 216)
- Demultiplexes data streams of up to 32 Gb/s (Option 232)/16.5 Gb/s (Option 216) into two data streams
- Tolerates small input signals with input sensitivity of 25 mVpp differential for clock data recovery and 70 mVpp differential for demultiplexing
- Provides aux clock with intrinsic random jitter as low as 100 fs RMS for accurate measurements
- Upgrades path for existing BERTs
- Enables easy operation and remote control through USB 2.0 and LAN connections, and standalone graphical user interface

## Characterize next-generation receivers and transmitters

The N4877A clock data recovery and demultiplexer 1:2 operates from 50 Mb/s to 32 Gb/s. The wide data-rate range allows testing of emerging standards like 100 GbE and 32GFC, while covering existing lower speed standards. A lower rate option operating up to 16.5 Gb/s, is ideal for 16GFC as well as computer standards like USB 3.0, SATA, SAS, SD UHS-II and PCIe including the emerging 16 GT/s generation.

## Recover clocks or clean-up clocks

The N4877A provides clock signals for BERTs or oscilloscopes when access to appropriate clock signals from the device under test (DUT) is not possible. But it can also act as a clean-up PLL for existing clocks with excessive intrinsic jitter to allow accurate measurements.

## Measure the real performance of clockless devices

Accurate transmitter measurements are possible because of low intrinsic jitter, paired with tunable loop bandwidth, selectable peaking and good sensitivity.

The N4877A's auxiliary clock output provides ultra-low intrinsic random jitter of less than 100 fs RMS, making it the ideal companion for sampling scopes equipped with a precision time base.

## Simplify receiver testing of high-speed devices

Receiver testing is easier because of software-controlled swappable demultiplexer outputs and a jitter tolerance test mode.

The N4877A clock data recovery and demultiplexer 1:2 is the counterpart to the N4876A multiplexer 2:1 and complements Keysight's J-BERT- and ParBERT-based receiver test solutions for data rates between 12.5 Gb/s and 28.4 Gb/s.

Cable kits specifically designed to maintain phase relationship between recovered clock and data are available for J-BERT N4903B.

## Easily control all settings

The N4877A's settings can be controlled through its rear-panel USB connection and a standalone user interface that runs on a Microsoft Windows® PC. The software can be installed on instruments running Windows XP® or Windows 7®.

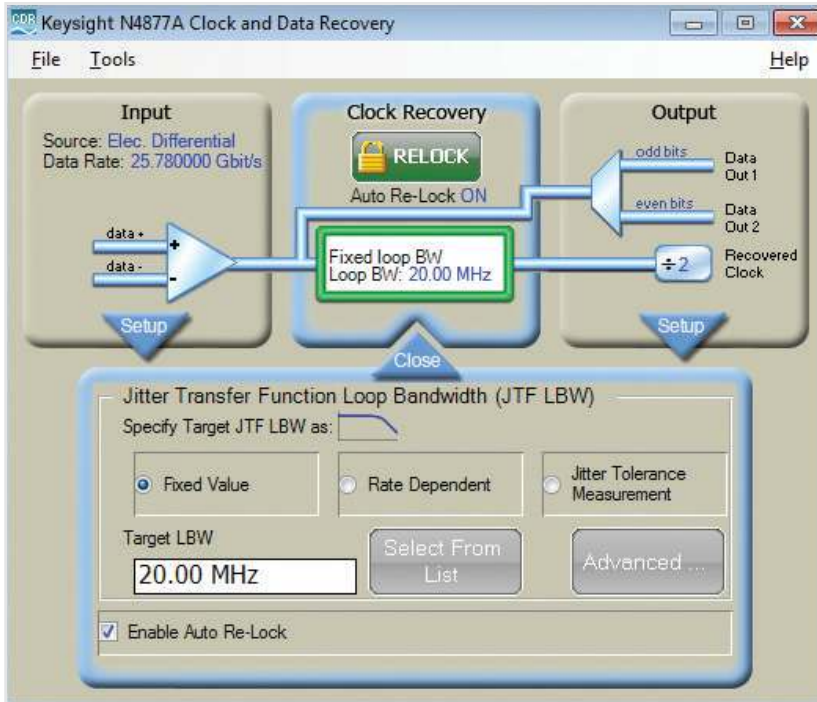


Figure 4. The intuitive graphical user interface is used to set expected data rate, change loop behavior, select output clock dividers and swap the demultiplexer outputs of the N4877A.

Support multiple applications with the N4877A

Application example: receiver testing with J-BERT N4903B N4903B high-performance serial BERT for 25 Gb/s

The N4877A clock data recovery and demultiplexer 1:2 can be used in a variety of applications. The following examples present typical use cases for clock data recovery in receiver and transmitter testing.

100 GbE, 32GFC, CEI and InfiniBand reach data rates beyond 25 Gb/s. The N4877A clock data recovery and demultiplexer is used in combination with the J-BERT N4903B and N4876A multiplexer for receiver testing of high-speed devices up to 28.4 Gb/s. In the example below, the N4877A recovers required sub-rate clocks and demultiplexes the 25 Gb/s data stream, enabling the J-BERT error detector to measure the bit-error-ratio during receiver sensitivity or jitter tolerance testing.

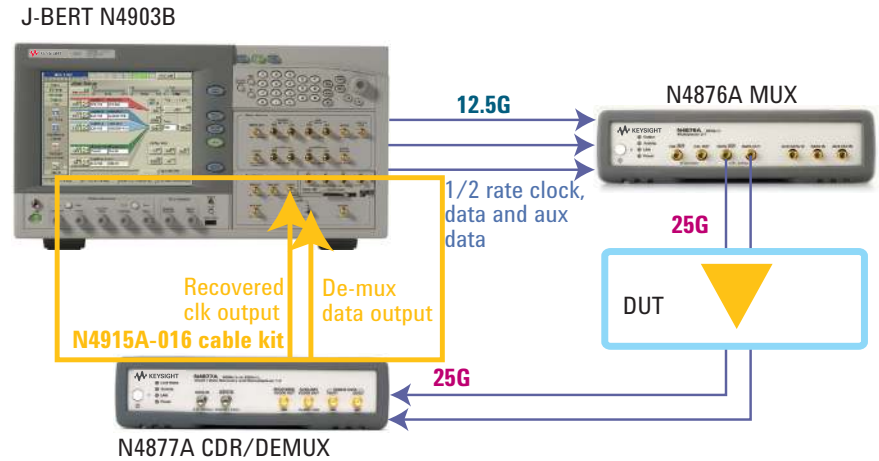


Figure 5. Setup for jitter tolerance characterization of a 28 Gb/s receiver. Cable kit N4915A-016 ensures the phase relationship between recovered clock and demultiplexed data.

Application example: clock recovery for sampling scope with high-bandwidth sampling heads and precision time base

Sampling scopes are the ideal choice for transmitter characterization when high-bandwidth, low noise floor and low intrinsic jitter are required. The N4877A, with its ultra-low jitter auxiliary clock output, provides a clean sine wave for a precision time-base module enabling the most accurate measurements. The main recovered clock output, with its divide stages, triggers the front panel trigger input.

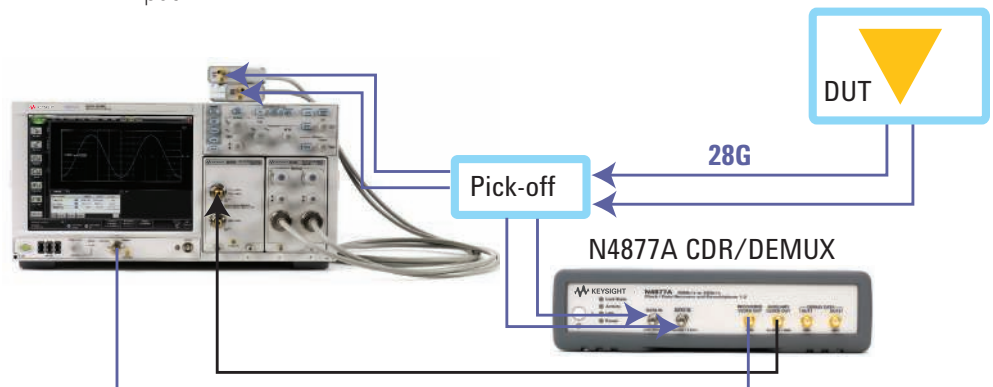


Figure 6. The setup for characterization of a 28 Gb/s high-bandwidth, low intrinsic jitter transmitter. For maximum performance the N4915A-015 pick-off kit is recommended.

Application example:  
28G data source with very low random jitter

The N4877A can be used as a cleanup PLL whenever a clean clock is required, such as for a 28 Gb/s data source with very low intrinsic random jitter (RJ). In the setup shown below, the N4877A cleans up the clock derived from the J-BERT N4903B to around 250 fs RJ RMS. This clock is used by the N4876A multiplexer to generate a data signal with very low RJ. The precision time base gets a very clean clock signal from the auxiliary clock out of the N4877A. The front panel trigger for the scope is provided by the J-BERT N4903B.

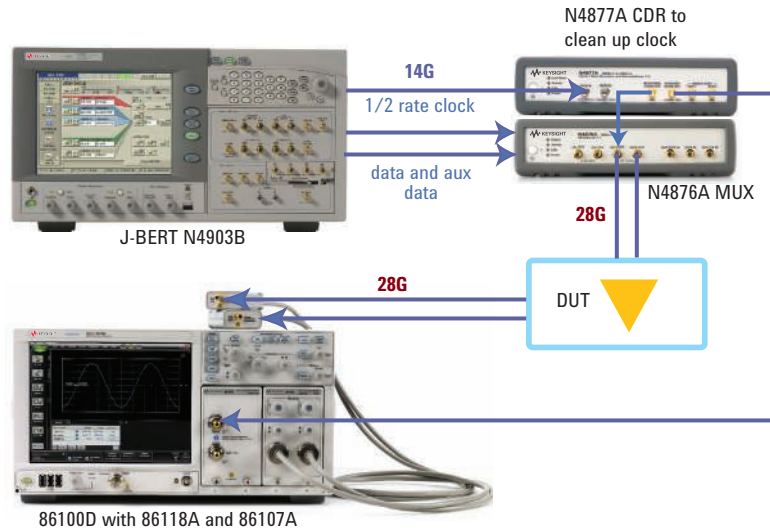


Figure 7. The N4877A is used to reduce random jitter for precision clocking.

Application example:  
27G testing with ParBERT

In combination with a multi-channel BERT system like the 81250 ParBERT, the N4877A clock data recovery and demultiplexer enables full-rate sampling up to 27 Gb/s. The CDR follows jitter within the range of its loop settings, while demultiplexing the incoming data stream into an even and odd bit stream. A ParBERT error detector (ED) clock group with two 13.5 Gb/s error detector modules analyzes every bit up to data rates of 27 Gb/s. The clocking for ParBERT's ED clock group is provided by the recovered clock of the N4877A.

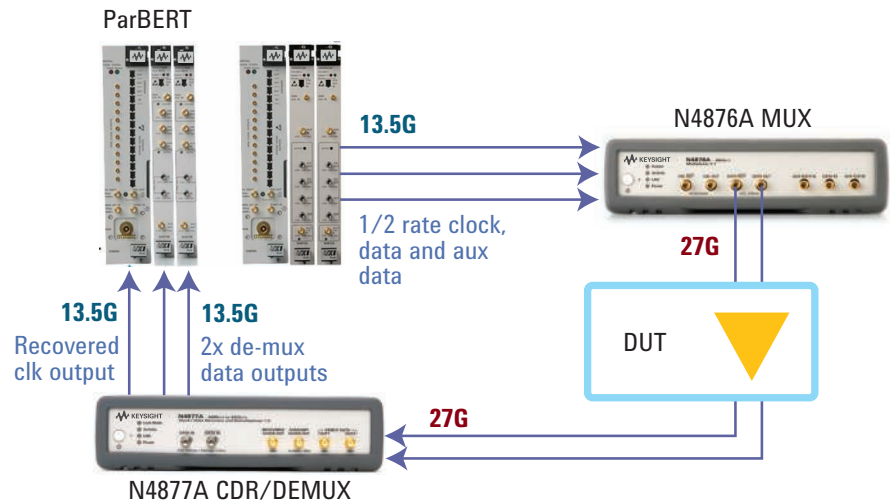


Figure 8. The ParBERT-based 27G test setup can be scaled for multi-lane testing by adding generators, analyzers, N4876As and N4877As.



## Specifications for N4877A



Figure 9. 2.4 mm (f) data signal inputs and SMA clock/data outputs on the front panel of the N4877A clock data recovery and demultiplexer 1:2.

### N4877A specifications

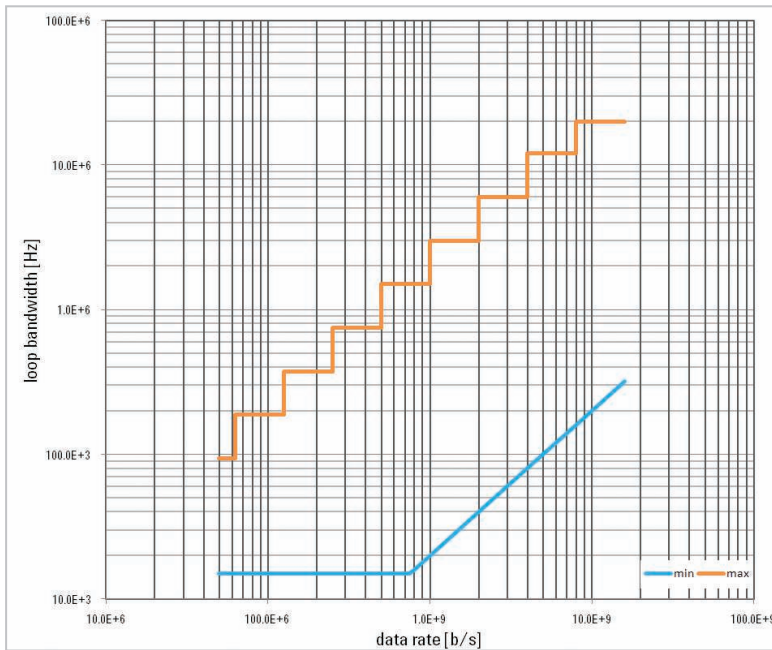
#### Data inputs

Input range	Option 232: Specified range: 380 Mb/s to 28.4 Gb/s Over programming range: 50 Mb/s to < 380 Mb/s and > 28.4 Gb/s to 32 Gb/s <sup>4</sup>
	Option 216: Specified range: 380 Mb/s to 16.5 Gb/s Over programming range: 50 Mb/s to < 380 Mb/s
Connector	2.4 mm (f)
Interface	Differential or single-ended, AC coupled, 50 $\Omega$ ; unused input must be terminated with 50 $\Omega$
Input voltage window/ max amplitude	-2.2 V to 3.2 V/2 V <sub>pp</sub> , max
Input sensitivity	25 mV single ended or differential to gain lock <sup>2</sup> , typical 70 mV single ended or differential for Demultiplexer @ BER 10 <sup>-12</sup> <sup>3</sup> , typical
Min. transition density	20% <sup>1</sup>

#### Recovered clock output

Connector	SMA (f)
Interface	Single-ended, AC coupled, 50 $\Omega$
Output voltage	350 mV <sub>pp</sub> , typical
Output frequency	16 GHz, max
Output dividers	User definable, available dividers are: 1 up to 16 Gb/s 2, 4, 8, 16 over full data-rate range





#### Loop bandwidth range

##### Data rate

50 Mb/s to 62.5 Mb/s  
 > 62.5 Mb/s to 125 Mb/s  
 > 125 Mb/s to 250 Mb/s  
 > 250 Mb/s to 500 Mb/s  
 > 500 Mb/s to 1.0 Gb/s  
 > 1.0 Gb/s to 2.0 Gb/s  
 > 2.0 Gb/s to 4.0 Gb/s  
 > 4.0 Gb/s to 8.0 Gb/s  
 > 8.0 Gb/s to 32 Gb/s

#### Max loop bandwidth

93.8 kHz  
 187.5 kHz  
 375.0 kHz  
 750.0 kHz  
 1.5 MHz  
 3.0 MHz  
 6.0 MHz  
 12.0 MHz  
 20.0 MHz

##### Data rate

50 Mb/s to 750 Mb/s  
 > 750 Mb/s to 32 Gb/s

#### Min loop bandwidth

15 kHz  
 (data rate)/(5000 b)

Peaking	Up to 4 peaking settings
Tracking range, including SSC	0.5% deviation, typical
Clock output jitter	400 fs RMS for data rates < 2.5 Gb/s, typical 250 fs RMS for data rates ≥ 2.5 Gb/s, typical

#### Auxiliary clock output

Connector	SMA (f)
Interface	Single-ended, AC coupled, 50 Ω
Output voltage	800 mV <sub>pp</sub> , typical
Output frequency	4 GHz to 8 GHz
Output jitter	< 100 fs RMS, typical

#### Data out 1 & 2

Connector	SMA (f)
Interface	Single-ended, AC coupled, 50 Ω
Data output voltage	350 mV <sub>pp</sub> , typical
Demultiplexing ratio	1:2
Data output jitter	5 ps pp, typical measured @ 14.2 Gb/s using a 1100 pattern
Skew: recovered clock to demux data out	644 ps, typical



Figure 11. USB and LAN connection are located at the back of the Keysight N4877A clock data recovery and demultiplexer 1:2.

### Rear panel

Connectors rear panel                    USB; LAN; IEC power connector

### General characteristics for N4877A

Power consumption	100–240 V, ~50/60 Hz, 90 VA, max
Operating temperature	10 °C to 40 °C
Storage temperature	–40 °C to 70 °C
Operating humidity	95% relative humidity, non-condensing
Storage humidity	50% relative humidity
Physical dimensions (W x H x D)	Bench top with bumper: 228 x 59 x 360 mm (9.0 x 2.3 x 14.2 in)
Rack mount without bumper	1/2 x 19" width, 1U height: 213 x 44.5 x 360 mm (8.4 x 1.8 x 14.2 in)
Weight net	2.9 kg (6.4 lb)
Weight shipping	5.5 kg (12.1 lb)

### Regulatory standards

Safety	IEC61010-1:2010, EN61010-1:2010, CAN/CSA-C22 No. 61010-04, UL 61010-1:2004
EMC	IEC61326-1:2005, EN61326-1:2006
Quality management	ISO 9004, ISO 14001

### Remote control interface

Connectivity	USB 2.0, LAN, rear panel
Programming language	Command line programming interface, SCPI
Standalone user interface	Color, graphical user interface
System requirements	Operating system: Microsoft Windows XP, SP3 (32 bit), or Vista SP2 (32 and 64 bit), or Windows 7 SP1 (32 and 64 bit) Microsoft .NET 2.0 SP2

1. The longest run of consecutive bits is dependent on data rate and loop bandwidth. Characteristic consecutive identical bits (CID): 150.
2. If the N4915A-015 pick-off kit is used on N4877A inputs, the 14 dB loss needs to be taken into account. Sensitivity with the N4915A-015 pick-off kit for CDR is 175 mV differential, typical.
3. If the N4915A-015 pick-off kit is used on N4877A inputs, the 14 dB loss needs to be taken into account. Sensitivity with the N4915A-015 pick-off kit for the demultiplexer is 350 mV differential, typical.
4. Sensitivity might be decreased for data rates above 28.4 Gb/s

## Keysight N1075A Optical Pick-Off/Converters



Figure 12. N1075A optical/pick-off converter for multimode and single-mode Option M14 to > 16 Gb/s (top) and single-mode up to 32 Gb/s Option S32 (bottom)

### Accurate, Convenient Solution for Recovering Clock Signals from High-Speed Optical Communication Signals

- Provides an easy method for using the N4877A clock recovery solution with optical signals
- Extracts a portion of the optical test signal using a built-in coupler. Main optical signal returned to the front panel
- Converts the tapped optical signal to an electrical signal compatible with the N4877A
- Operates with both multimode and single-mode optical signals

Verify the compliance of next-generation transmitters

Many communications standards specify the use of a timing reference recovered from the DUT for transmitter compliance test. Clock recovery with an adjustable loop bandwidth provides an important jitter filtering response that emulates system response and can provide an important margin in eye-mask tests. The N1075A extends the clock recovery performance of the N4877A to provide this capability for optical test.

Test system-level optical waveforms and BER

When an optical transmitter is deployed in a communication system, a timing reference for oscilloscope triggering may not be available and must be derived from the signal-under-test. BERT systems typically only accept electrical signals. The N1075A can be used to derive an electrical signal from an optical input, while passing the main optical signal to the 86100 DCA. The N4877A generates a clock trigger for oscilloscope synchronization. For BER test, the N1075A/N4877A can provide electrical clock and data to the BERT-error-detector derived from an optical signal.

Analyze live traffic of optical communications networks

The N1075A is placed in an active communications link. The coupled signal is converted by the N1075A into an electrical signal that can be monitored with a real-time oscilloscope for protocol and pattern analysis.

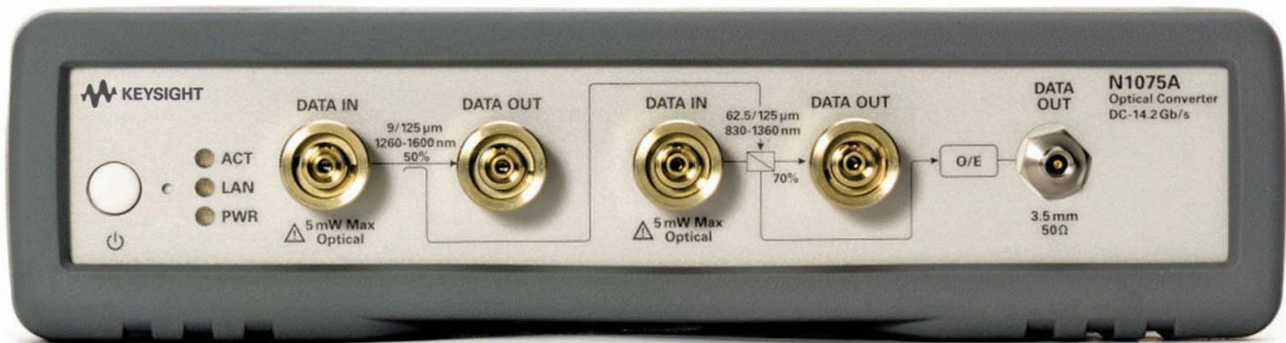


Figure 13. A front panel view of the Keysight N1075A M14 optical pick-off/converter.

# Specifications for N1075A

N1075A-M14 Specifications	
Internal split ratio (to OE / to front panel)	30/70 multimode path 50/50 single-mode path
Data rate range	DC coupled, to > 16 Gb/s (optical-to-electrical conversion is purely analog and rolls off but continues to operate above 16 Gb/s)
Insertion loss	4.5 dB 850 nm multimode path 4.5 dB 1550 nm single-mode path
Input return loss	16 dB multimode path 25 dB single-mode path
Wavelength range	830 nm to 1360 nm multimode path 1250 nm to 1650 nm single-mode path
Noise equivalent power	10 $\mu$ W (13 dB SNR or 200 $\mu$ W required to achieve lock with N4877A. Higher powers required above 16 Gb/s)
Data input/output connectors	FC/PC 62.5/125 $\mu$ m multimode optical FC/PC 9/125 $\mu$ m single-mode optical 3.5 mm electrical (output only)
Optical-to-electrical conversion gain (responsivity is reduced above 16 Gb/s)	60 V/W minimum multimode path 95 V/W minimum single-mode path



Figure 14. A front panel view of the Keysight N1075A M14 optical pick-off/converter.

N1075A-S32 Specifications	
Internal split ratio (to OE / to front panel)	50/50 single-mode
Data rate range	DC coupled to 32 Gb/s
Insertion loss	4.5 dB 1550 nm single-mode
Input return loss	25 dB single-mode
Wavelength range	1300 nm to 1620 nm single-mode
Noise equivalent power	7.5 $\mu$ W typical (13 dB SNR or 150 $\mu$ W assures lock with N4877A. Higher powers required above 16 Gb/s)
Data input/output connectors	FC/PC 9/125 $\mu$ m single-mode optical 2.4 mm electrical (output only)
Optical-to-electrical conversion gain (Responsivity is reduced above 16 Gb/s)	110 V/W minimum





Figure 14. A rear panel view of the Keysight N1075A optical pick-off/converter.

#### General characteristics for N1075A M14 and S32

Power consumption	100-240 V, ~47 Hz to 63 Hz, 80 VA max
Operating temperature	10 °C to 40 °C
Maximum relative humidity	80% for temperatures up to 31 °C decreasing linearly to 50% relative humidity at 40 °C Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of storage, transportation and end-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test methods are aligned with IEC 60068-2 and levels are similar
Storage temperature	-40 °C to 70 °C
Max. altitude	Up to 2000 m
Physical dimensions (W x H x D)	Bench top with bumper: 228 x 59 x 360 mm (9.0 x 2.3 x 14.2 in)
Rack mount without bumper	1/2 x 19" width, 1U height: 213 x 44.5 x 360 mm (8.4 x 1.8 x 14.2 in)
Weight net	-M14: 3.06 kg (6.75 lb) -S32: 2.72 kg (6 lb)
Weight shipping	5.7 kg (12.5 lb)

#### Regulatory standards

Safety	IEC61010-1:2001, EN61010-1:2001, CAN/CSA-C22 No. 61010-04, UL 61010-1:2004
EMC	IEC61326-5-1:2005, EN61326-2-1:2006
Quality management	ISO 9004, ISO 14000

## Keysight N1070A Optical Clock Recovery Solution



Figure 16. N1070A optical clock recovery solution M14/216 for multimode and single-mode to > 16 Gb/s



Figure 17. N1070A optical clock recovery solution S32/232 for single-mode up to 32 Gb/s

### A High-Performance, Convenient Solution for Deriving Clock and Synchronization from Optical Digital Communication Signals

- Bundles the N4877A clock data recovery instrument with the N1075A optical pick-off/converter
- Optional N1027A cabling accessories maintain correct phase relationships between trigger and samples in 86100 oscilloscope applications
- Provides a simple 86100 DCA configuration when both a precision time base and clock data recovery are required



## Achieve accurate waveform jitter analysis

When signals are measured with an oscilloscope that is triggered with a recovered clock, accurate jitter measurements become dependent on maintaining the correct phase relationship between trigger events and sampling. A common example is when there are large jitter components at discrete frequencies common with receiver stress test signals. For example, if a large sinusoidal jitter component is present and the oscilloscope is triggered at one extreme of the jitter deviation, but the sample is acquired at the opposite extreme, the apparent displayed jitter will be double the actual value. Correct phase relationships are maintained through specific cabling between the N1075A, N4877A, and 86100. These cables are provided with the N1070A bundle by ordering the appropriate N1027A accessory cable kit. The N1027A-M14 and N1027A-S32 configurations each have a unique set of cables that provide balance between the trigger and sampling paths.

## Configure an 86100 waveform test system for the highest optical waveform accuracy

The 86100 digital communications analyzer is the industry standard for optical waveform analysis. When analyzing very high data-rate low jitter signals, the 86100 is typically configured with the 86107A precision time base module. When triggering the 86100 with a recovered clock, the ultra-low jitter output from the N1070A/N4877A auxiliary output provides an ideal signal for any version of the 86107A. As an added benefit, the N1070A does not require space in the 86100 mainframe.

## Expected performance of the N1070A

The N1070A optical clock recovery solution is based on the N4877A clock data recovery instrument and the N1075A optical coupler/converter. Specifications are based on the performance of these two individual instruments. Performance of the combined instruments is not warranted, as the solution is not tested as a combined system.

In general, the signal quality and strength required to achieve a phase-locked condition and generate a clock is much less than what would be considered appropriate for an eye-mask test or for parametric analysis of an eye diagram. The N1075A-M14 system is rolling off above 16 Gb/s. However, if the signal power is large, phase lock can be achieved at 25 and 28 Gb/s. The following information provides useful parameters to help determine appropriate signal-level performance for proper operation.

## Operating conditions

### Minimum optical modulation power to achieve lock (at the input of the N1075A)

#### N1070A with N1075 M14

850 nm multimode path	-9 dBm @ 10 Gb/s
	-9 dBm @ 14 Gb/s
	-3 dBm @ 25 Gb/s
	-1 dBm @ 28 Gb/s

1550 nm single-mode path	-10 dBm @ 10 Gb/s
	-9 dBm @ 14 Gb/s
	-5 dBm @ 25 Gb/s
	-1 dBm @ 28 Gb/s

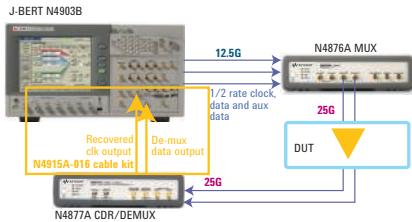
#### N1070A with N1075 S32

1550 nm single-mode path	-15 dBm @ 10 Gb/s
	-14 dBm @ 14 Gb/s
	-12 dBm @ 28 Gb/s
	-10 dBm @ 32 Gb/s

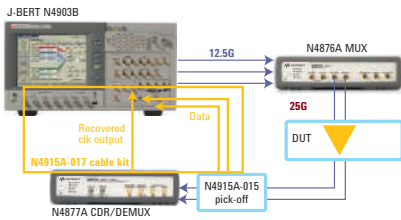
Ordering information  
N4877A clock data recovery  
and demultiplexer 1:2

Includes: 2x adapters 2.4 mm (m) to 3.5 mm (f), 4 x 50 Ω termination SMA (m), USB cable, ROHS addendum, commercial calibration report and certificate, CD with software, user guides, and a hard copy Getting Started Guide.

Description	Model number
Clock data recovery and demultiplexer 1:2	N4877A
Data rate range 50 Mb/s to 32 Gb/s	N4877A-232
Data rate range 50 Mb/s to 16.5 Gb/s	N4877A-216
High bandwidth pick-off kit for N4877A	N4915A-015
<b>Includes:</b> A matched pair of high-bandwidth 14 dB pick-offs 2.4 mm (m) – 3.5 mm (f) – 2.4 mm (f) 14 dB / 20% output to N4877A inputs 2 x 2.4 mm (f) to 2.4 mm (f) adapters 2 x 3.5 mm (m) to 2.4 mm (m) adapters direct mount to N4877A inputs	
Cable kit for N4877A CDR and demux to N4900 series BERT error detector	N4915A-016
<b>Remark:</b> This cable kit is recommended if the N4877A CDR and demultiplexer functions are used in combination with a N4900 Series BERT. The cable kit ensures correct data clock delay.	
<b>The cable kit contains:</b> 1x SMA (m) to SMA (m) cable for clock connection 1x SMA (m) to 2.4 mm (m) cable for demultiplexer out to N4900 series BERT error detector connection	
Cable kit for N4877A CDR and demux to N4900 series BERT error detector	N4915A-017
<b>Remark:</b> This cable kit is recommended when the N4877A CDR function but not the demultiplexer function is used in combination with a N4900 Series BERT. The cable kit ensures correct data clock delay when used with the N4915A-015 high bandwidth pick-off set.	
<b>The cable kit contains:</b> 1x SMA (m) to SMA (m) cable for clock connection 1x matched pair 2.4 mm (m) to 2.4 mm (m) cable for pick-off (N4915A-015) out to N4900 Series BERT error detector connection	
Cable kit: 2.4 mm matched cable pair	N4910A
Adapter 3.5 mm (f) to 2.4 mm (m)	N4911A-002
Termination SMA (m) 50 Ω	N4911A-004
Termination 2.4 mm (m) 50 Ω	N4912A
Power divider, DC to 26.5 GHz, 3.5 mm (f) – 3.5 mm (f) – 3.5 mm (f)	11636B
Power divider, DC to 50 GHz, 2.4 mm (f) – 2.4 mm (f) – 2.4 mm (f)	11636C
Adapter 2.4 mm (m) to 3.5 mm (m), DC to 26.5 GHz	11901A
Adapter 2.4 mm (m) to 2.4 mm (m), DC to 50 GHz	11900A
Rack-mount kit	N7744A-100
Warranty and calibration service	R1280



N491A-016 cable kit is orange in above diagram



N491A-017 cable kit is orange in above diagram

Ordering information  
N1075A optical  
pick-off/converter

Included accessories: functional test report; ROHS addendum, FC/PC optical connector adapters.

Description	Model number
Optical pick-off/converter	N1075A
Single-mode and multimode > 16 Gb/s	N1075A-M14
Single-mode up to 32 Gb/s	N1075A-S32
Rack-mount kit	E5810A-100
Warranty and calibration service	R1280

Ordering information  
N1070A optical clock  
recovery solution

Included accessories: : All standard accessories included with the N4877A and N1075A and the electrical cable and adapters to connect the N1075A electrical output to the N4877A data input

Description	Model number
Optical clock recovery solution	N1070A
Customer selects N4877A-216 or N4877A-232	See N4877A details
Customer selects N1075A-M14 or N1075A-S32	See N1075A details
Includes phase matching cable kit for N1075A-M14 + N4877A	N1027A-M14
Includes phase matching cable kit for N1070A-S32 + N4877A	N1027A-S32
Rackmount kit for one or two instruments	N7744A-100
Warranty and calibration service (for individual N4877A and N1075A instruments and not as a combined system)	R1280

Other clock data recovery  
products

Next to the N4877A clock data recovery and demultiplexer 1:2, Keysight offers a selection of other electrical clock data recovery products

Description	Model number
13 Gb/s clock data recovery unit 622 Mb/s to 13.5 Gb/s	N4982A-R13
26 Gb/s clock recovery module	N4982A-R19
25.8 Gb/s / 28 Gb/s / 31 Gb/s clock data recovery module	N4982A-R25
28 Gb/s clock data recovery module	N4982A-R28
40 Gb/s clock data recovery module	N4982A-R40

## Related Literature

Title	Publication number
Instrumentation-Grade Clock Recovery Solutions to 32 Gb/s, Brochure	5990-9933EN
Keysight 86100D Wide-Bandwidth Oscilloscope, Brochure	5990-5822EN
Infiniium 90000 X-Series Oscilloscopes 16-32 GHz True Analog Bandwidth, Data Sheet	5990-5271EN
Infiniium DSO90000 Series High-Performance Oscilloscopes, Data Sheet	5989-7819EN
J-BERT N4903B High-Performance Serial BERT, Data Sheet	5990-3217EN
N4876A 28 Gb/s Multiplexer 2:1, Data Sheet	5990-5247EN
ParBERT 81250 System, Technical Overview	5968-9188E
Tips and Techniques for Accurate Characterization of 28 Gb/s Designs, Application Note	5990-9784EN
Error Detection Up to 28.4 Gb/s During Receiver Test with Keysight J-BERT N4903B Using Under-Sampling Techniques, Application Note	5990-6239EN
N4960A Serial BERT 32 and 17 GB/s, Data Sheet	5991-0712EN

## Specification assumptions

Non-warranted values are described as typical.

All specifications are valid in the range from 5 °C to 40 °C except if otherwise stated ambient temperature after a warm-up phase of 30 minutes.

If not otherwise stated, all inputs and outputs need to be terminated with 50  $\Omega$  to ground.

All specifications, if not otherwise stated, are valid using the recommended cable set N4910A (2.4 mm, 24" matched pair).

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