

Keysight Technologies
M8085A MIPI Receiver Test Solutions

Data Sheet
Version 2.0



Introduction

The M8085A is a software plug-in for M8070A Bit Error Ratio Test system software within the M8000 series of BER test solutions. The M8085A software plug-in controls an M8190A or M8195A Arbitrary Waveform Generator (AWG) to create C-PHY and D-PHY standard conformant test signals. Depending on the provisions for error detection implemented in the DUT receiver (RX) the plug-in provides the option to connect to your DUT built-in receiver via the so-called IBERReader interface, which is based on a user provided DLL, to read the bit error counter and display the result in the M8085A user interface.

Key benefits

- Fast characterization of digital C-PHY and D-PHY receivers through easy test signal generation
- Editor enabling set-up of all PHY-parameters in application terms
- Reliable and automated calibration of signal parameters
- Complete and conformant RX test procedures for single lane enabling automated, unattended test
- Can be operated manually or through program control via customer or N5990A Keysight test sequencer

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MIPI Receiver Test Solutions

The next level of integration

The M8000 Series of BER test solutions for digital RX characterization with its modular AXI-HW architecture and its Plug In SW-concept allows composing the required BERT consisting of Pattern Generator (PG) and Error Detector (ED) building blocks using a Keysight M819x AWG as PG and the M8070A System Software. The M8070A SW furthermore hosts the application specific test automation SW Plug-In M8085A as depicted below in Figure 2 below, which in turn hosts the IBERReader interface providing the connection to the error detector that needs to be provided by the DUT.

The functionality is visualized in the (SW-) block diagram

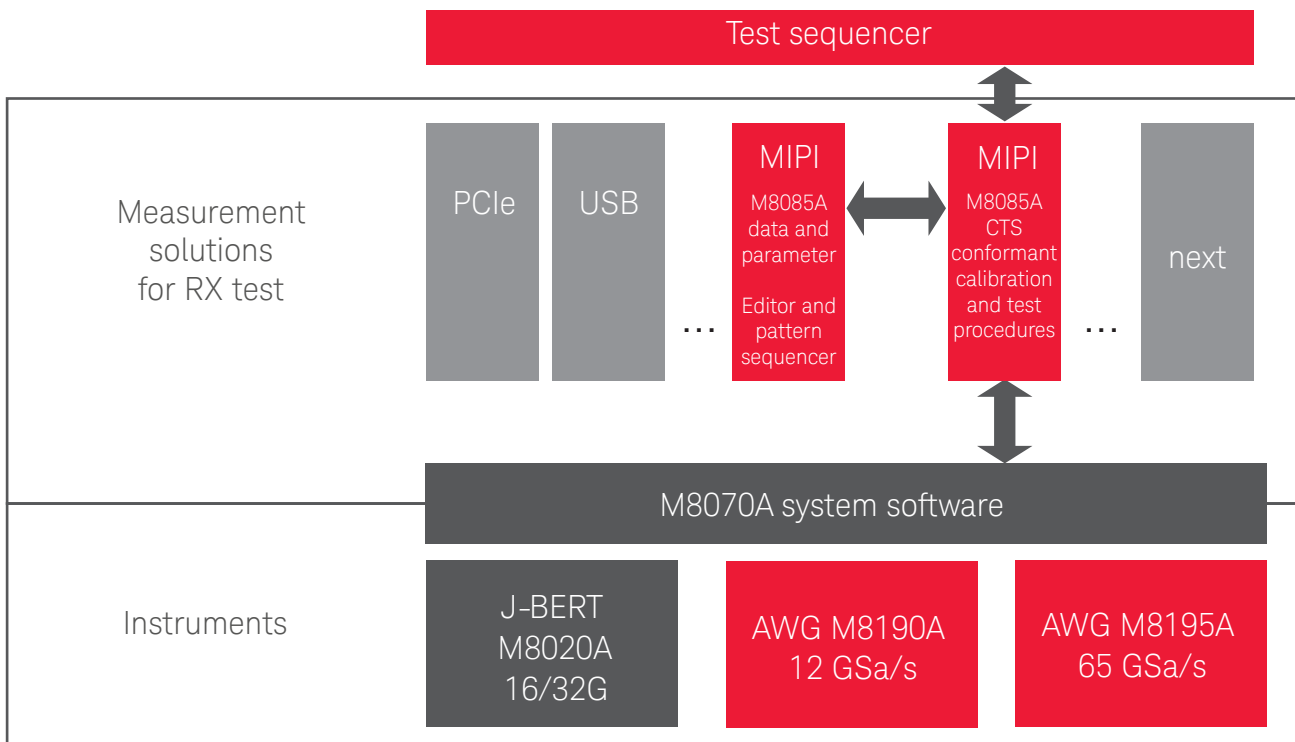


Figure 2. Architecture of application specific solutions within the M8000 System.

Building blocks of a complete RX test

An RX test is used to determine an RX's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing

- A Bit Error Ratio Tester's (BERT) Pattern Generator (BERT PG) is used to emulate a system's TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.
- This signal has to be calibrated according to the specification / conformance test suite (CTS)
- The RX is set into test mode and the input of the RX under test is stimulated with the calibrated test signal
- Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

These tasks are depicted in the functional block diagram Figure 3 below. The functionality is delivered by separate SW blocks allowing the user to tailor the solution according to his needs.

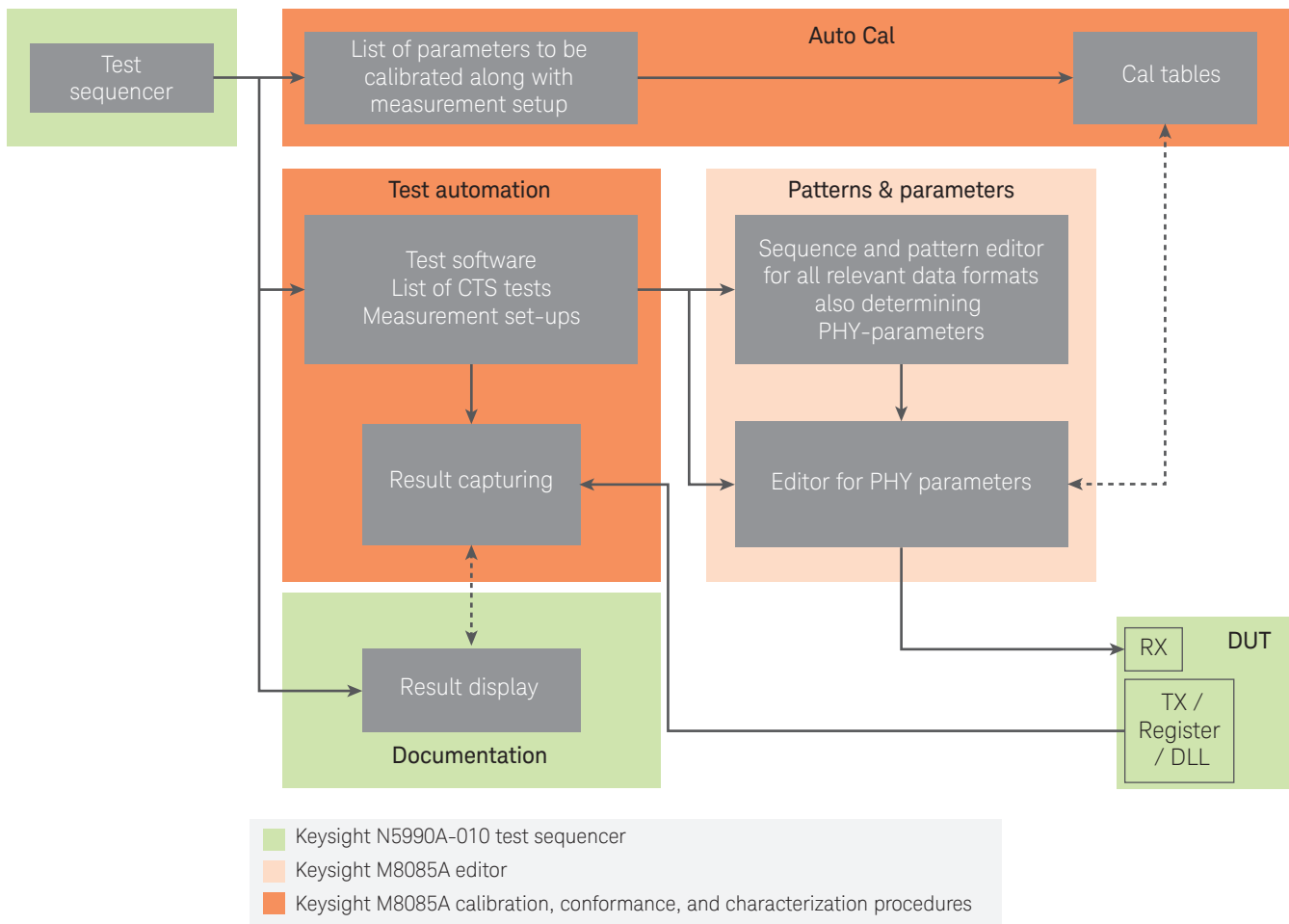


Figure 3. Building blocks of an RX Test and Related SW Products using Plug Ins for the M8000 System SW M8070A.

1. Editors allow direct setup of PHY parameters and data content (local from GUI or remote under program control via SCPI commands)
2. Automated calibration, conformance and characterization procedures can be started individually from GUI or a remote program
3. In case the customer does not want to generate his own remote control program or use his own test sequencer the test sequencer from the Keysight N5990A Test Automation Software Platform provides complete automated control of all the calibration and tests.

M8085A Products and Options

The M8085A addresses mobile applications. Products M8085Cxx and M8085Dxx are addressing C-PHY and D-PHY standard respectively. The SW is available as a perpetual, Transportable or Network license.

Product No.	Option	Description
M8085CE1A	-1TP	MIPI C-PHY 1.2 Editor for M819xA AWG, Transportable, Perpetual License
	-1NP	MIPI C-PHY 1.2 Editor for M819xA AWG, Network/Floating, Perpetual License
M8085CC1A	-1TP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License
	-1NP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License
M8085CUEA	-1TP	Upgrade C-PHY Editor from M8085A-CT1 to C-PHY 1.2, Transportable, Perpetual License
	-1NP	Upgrade C-PHY Editor from M8085A-CN1 to C-PHY 1.2, Network/Floating, Perpetual License
M8085CUCA	-1TP	Upgrade C-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-CT1 and M8085A-CTA to C-PHY 1.2, Transportable, Perpetual License
	-1NP	Upgrade C-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-CN1 and M8085A-CNA to C-PHY 1.2, Network/Floating, Perpetual License
M8085DE1A	-1TP	MIPI D-PHY 2.0 Editor for M819xA AWG, Transportable, Perpetual License
	-1NP	MIPI D-PHY 2.0 Editor for M819xA AWG, Network/Floating, Perpetual License
M8085DC1A	-1TP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License
	-1NP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License
M8085DUEA	-1TP	Upgrade D-PHY Editor from M8085A-DT1 to D-PHY 2.0, Transportable, Perpetual License
	-1NP	Upgrade D-PHY Editor from M8085A-DN1 to D-PHY 2.0, Network/Floating, Perpetual License
M8085DUCA	-1TP	Upgrade D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DT1 and M8085A-DTA to D-PHY 2.0, Transportable, Perpetual License
	-1NP	Upgrade D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DN1 and M8085A-DNA to D-PHY 2.0, Network/Floating, Perpetual License

C-PHY and D-PHY are used for camera (CSI) and Display (DSI) applications. Both can appear as single or multi-lane applications. Which SW option and which AWG module is required for which flavor is listed below:

MIPI Type	Addressable numbers	Usable HW modules	Applicable SW Products
D-PHY	1	M8190A, M8195A	M8085DE1A, M8085DC1A, M8085DUEA, M8085DUCA
	1,2,4	M8195A	M8085DE1A, M8085DC1A, M8085DUEA, M8085DUCA
C-PHY	1	M8190A, M8195A	M8085CE1A, M8085CC1A, M8085CUEA, M8085CUCA
	1,2,4	M8195A	M8085CE1A, M8085CC1A, M8085CUEA, M8085CUCA

Standards are continuously improved addressing evolving needs e.g. for higher bandwidth (BW) and/ or lower power etc. The table below shows, which options address which standard / CTS revisions.

MIPI Type	Addressed Standard / CTS-Revisions	Applicable SW Products
D-PHY	Up to 2.0	M8085DE1A, M8085DC1A, M8085DUEA, M8085DUCA
C-PHY	Up to 1.2	M8085CE1A, M8085CC1A, M8085CUEA, M8085CUCA

Benefits

Key features of the M8085A editor options

As already mentioned above, the test stimulus used for C-PHY and D-PHY application is created by the AWGs. These instruments generate their output signal from a vector memory that contains the digitized waveform information. Usually the waveform vectors must be generated by the user utilizing waveform synthesis tools such as MATLAB or equivalent. With the M8085A editor SW products, these instruments can be operated from the familiar user interface that the M8070A SW provides for the J-BERT M8020A - with the addition of application specific parameters as shown below in Figures 4 to 6 for the C-PHY or D-PHY applications.

The screenshot shows the M8085A GUI for C-PHY editor. The 'Data Pattern' section on the left includes options for Run Mode (Interrupted), Idle Voltage (300 mV), Mode (Pattern, Burst, Pure HS, Frames), HS Data (0xE7, 0xE7, 0xE7, 0xE7), and LP Data (0xE7, 0xE7, 0xE7, 0xE7). The 'Data Rates & Transition Times' section shows LP Data Rate (10 Mb/s), HS Data Rate (1 Gb/s), LP TT (2 ns), and HS TT (30 ps). The 'Parameters' table on the right is highlighted with a red box and contains the following data:

Protocol	CPHY1.Link
T3-PREPREP Duration	50.0 ns
T3-PREBEGIN	3333333
T3-PROGSEQ	
T3-PREEND	3333333
T3-SYRC	3444444
T3-POST	4444444
TX-HS-EXIT Duration	200.0 ns
TX-WAKEUP Duration	1.0000 ms
TX-DINT Duration	100.00 us

Annotations in the image include:

- Green box:** HS-pattern can be set up as
 - Hexadecimal data
 - C-PHY wire state or symbol value
 - Predefined PRBS
- Red box:** LP-pattern serial data
 - Hexadecimal data
- Red box:** Automatic transition between HS and LP using programmable protocol parameters

Figure 4 C-PHY editor showing GUI for Data set-up

The screenshot shows the M8085A GUI for C-PHY or D-PHY editor. The 'Data Pattern' section on the left includes options for Run Mode (Interrupted), Idle Voltage (300 mV), HS Sync Word (0xB8), and Protocol (CSI, DSI). The 'Data Rates & Transition Times' section shows LP Data Rate (10 Mb/s), HS Data Rate (1 Gb/s), LP TT (2 ns), and HS TT (8 ns). The 'Parameters' table on the right is highlighted with a red box and contains the following data:

Signal Levels	DPHY1.Lane
Lane	All
Signal	Both
LP High Level (V)	1.200 V

Annotations in the image include:

- Red box:** HSFreq: 158 MBit/s; Blocks: FrameStart: C000000,LP11E10880; Blanking: LP11E10880; Video: C2B"Raw10_256x200.dat",LP11E10880; FrameEnd: C010000,LP11E10880; Sequence: 1. FrameStart,1; 2. Blanking,1; 3. Video,100; 4. Blanking,2; 5. FrameEnd,1;
- Red box:** Automatic transition between HS and LP using programmable protocol parameters

Figure 5. C-PHY or D-PHY editor showing GUI for CSI or DSI data set-up

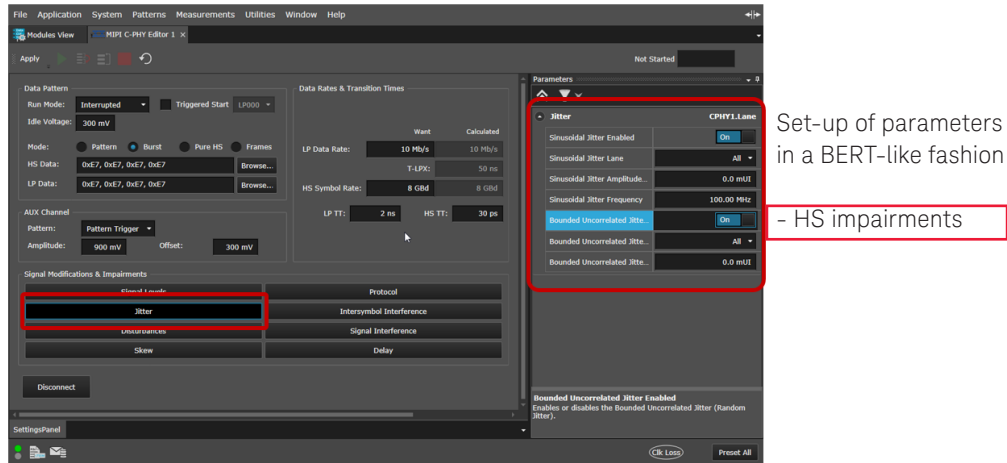


Figure 6. C-PHY or D-Phy editor showing GUI for LP-HS transition.

Key features of the M8085A calibration and test procedure options

A prerequisite for any RX test is to stimulate the RX with well-calibrated test signals. As the test set-ups often differ from those used to perform the factory calibration of the generators and influence the parameter values it is necessary to do an in-situ calibration. The Conformance Test Suites (CTS) for both C-PHY and D-PHY specify the different test set-ups and by this indirectly also the calibration procedures.

Furthermore, they contain quite a few tests to verify the conformance or characterize the margins of the respective HS and LP RXs, as well as tests verifying proper behavior during mode transitions. To unburden the user from having to study the CTS and maybe the specification itself and translate the insights into test set-ups, calibration and test procedures. Keysight provides the M8085CC1A and M8085DC1A containing these calibration, test and characterization procedures.

Below it is listed which tests are addressed by the above mentioned SW options.

List of tests C-PHY provided by M8085CC1A	
CTS SECTION 2: RX TIMERS AND ELECTRICAL TOLERANCES	
GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS	
- Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH)	√
- Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	√
- Test 2.1.3 – LP-RX Input Hysteresis (VHYST)	√
- Test 2.1.4 – LP-RX Minimum Pulse Width Response (TMIN-RX)	√
- Test 2.1.5 – LP-RX Input Pulse Rejection (eSPIKE)	√
GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS	
- Test 2.2.1 – LP-RX Initialization period (TINIT)	√
- Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value	√
- Test 2.2.3 – LP-RX Invalid/Aborted Escape Mode Entry	√
- Test 2.2.4 – LP-RX Invalid/Aborted Escape Mode Command	√
- Test 2.2.5 – LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	√
- Test 2.2.6 – LP-RX Escape Mode Unsupported/Unassigned Commands	√
GROUP 3: HS-RX VOLTAGE AND JITTER TOLERANCE REQUIREMENTS	
- Test 2.3.1 – HS-RX Amplitude Tolerance (VCPRX(DC), VIHHS, VILHS)	√
- Test 2.3.2 – HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)	√
- Test 2.3.3 – HS-RX Jitter Tolerance	√
GROUP 4: HS-RX TIMER REQUIREMENTS	
- Test 2.4.1 – HS-RX T3-TERM-EN Duration	√
- Test 2.4.2 – HS-RX T3-PREPARE Tolerance	√
- Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance	√
- Test 2.4.4 – HS-RX T3-PROGSEQ Tolerance	√
- Test 2.4.5 – HS-RX T3-POST Tolerance	√

List of tests D-PHY provided by M8085DC1A**CTS SECTION 2: RX TIMERS AND ELECTRICAL TOLERANCES****GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS**

- Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH) ✓
- Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (VIL) ✓
- Test 2.1.4 – LP-RX Input Hysteresis (VHYST) ✓
- Test 2.1.5 – LP-RX Minimum Pulse Width Response (TMIN-RX) ✓
- Test 2.1.6 – LP-RX Input Pulse Rejection (eSPIKE) ✓
- Test 2.1.7 – LP-RX Interference Tolerance (VINT and FINT) ✓
- Test 2.1.8 – LP-CD Logic Contention Thresholds (VIHCD and VILCD) ✓

GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS

- Test 2.2.1 – LP-RX Initialization period (TINIT) ✓
- Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value ✓
- Test 2.2.3 – Clock Lane LP-RX Invalid/Aborted ULPS Entry ✓
- Test 2.2.4 – Data Lane LP-RX Invalid/Aborted Escape Mode Entry ✓
- Test 2.2.5 – Data Lane LP-RX Invalid/Aborted Escape Mode Command ✓
- Test 2.2.7 – Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits ✓
- Test 2.2.8 – Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands ✓

GROUP 3: HS-RX VOLTAGE AND SETUP/HOLD REQUIREMENTS

- Test 2.3.1 – HS-RX Common Mode Voltage Tolerance (VCMRX(DC)) ✓
- Test 2.3.2 – HS-RX Differential Input High Threshold (VIDTH) ✓
- Test 2.3.4 – HS-RX Single-Ended Input High Voltage (VIHHS) ✓
- Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (VILHS) ✓
- Test 2.3.6 – HS-RX Common-Mode Interference 50MHz - 450MHz (Δ VCMRX(LF)) ✓
- Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450MHz (Δ VCMRX(HF)) ✓
- Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance ✓

GROUP 4: HS-RX TIMER REQUIREMENTS

- Test 2.4.1 – Data Lane HS-RX TD-TERM-EN Value ✓
- Test 2.4.2 – Data Lane HS-RX THS-PREPARE + THS-ZERO Tolerance ✓
- Test 2.4.3 – Data Lane HS-RX THS-SETTLE Value ✓
- Test 2.4.4 – Data Lane HS-RX THS-TRAIL Tolerance ✓
- Test 2.4.5 – Data Lane HS-RX THS-SKIP Value ✓
- Test 2.4.6 – Clock Lane HS-RX TCLK-TERM-EN Value ✓
- Test 2.4.7 – Clock Lane HS-RX TCLK-PREPARE + TCLK-ZERO Tolerance ✓
- Test 2.4.8 – Clock Lane HS-RX TCLK-SETTLE Value ✓
- Test 2.4.9 – Clock Lane HS-RX TCLK-TRAIL Tolerance ✓
- Test 2.4.10 – Clock Lane HS-RX TCLK-MISS Value ✓
- Test 2.4.11 – Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance ✓

Performing calibration and tests automatically

Figure 7 below shows how the M8085CC1A C-PHY or M8085DC1A D-PHY calibration procedure guides the user through the connections of the oscilloscope with the AWG and the DUT. The result of the automated calibration is displayed in graphical form as well as with numerical values listed in a table.

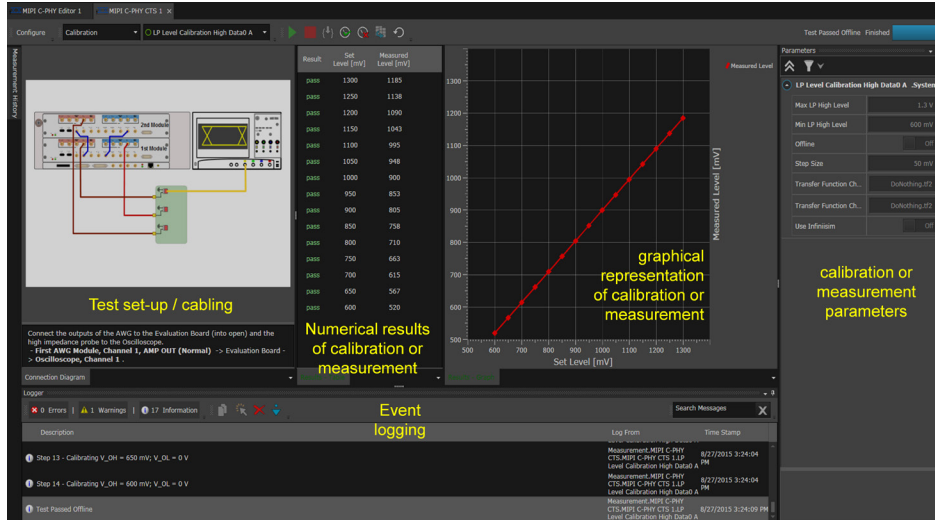


Figure 7. GUI of M8085CC1A / M8085DC1A. Calibration and test routines for C-PHY / D-PHY

Ordering a MIPI C-PHY Receiver Test Configuration

Complete n-Lane C-PHY Setup (HS, LP, and transitions, full compliance) using M8195A modules		1	3	4
Number of C-PHY lanes				
Option	Description	Quantity		
M8195A-BU1	AXIe Chassis: 5-slot with Integrated System Module plus Embedded Controller: Quad Core, 8GB RAM, 160 SSD, 2 GB/s	1	1	1
M8195A-004	Arbitrary Waveform Generator, 4 Channels, 65 GSa/s	1	3	4
M8195A-16G	Upgrade to 16 GSa Memory	1	3	4
M8195A-SEQ	Sequencer	1	3	4
M8197A	Synchronisation module for the M8195A	0	1	1
M8070A-OTP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	1	1
M8070A-ONP	System Software for M8000 Series of BER Test Solutions, Network License	0	0	0
M8070A-1TP	Device Control Interface	1	1	1
M8085CE1A-1TP	MIPI C-PHY 1.2 Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085CC1A-1TP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085CE1A-1NP	MIPI C-PHY 1.2 Editor for M819xA AWG, Network/Floating, Perpetual License	0	0	0
M8085CC1A-1NP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	0	0	0
N5990A-010	Bitifye Test sequencer for M8085A C-PHY Products	1	1	1
Complete 1-Lane C-PHY Setup (HS, LP, and transitions, full compliance) using M8190A modules		Quantity		
M8190A-BU1	Bundle 1 consisting of M9505A AXIe Chassis w/ 5 slots and M9536A Embedded PC Controller	1		
M8190A-001	Arbitrary Waveform Generator 1 Channel	1		
M8190A-002	Arbitrary Waveform Generator 2 Channel	1		
M8190A-02G	Upgrade from 128Msa to 2GSa Memory/Channel	3		
M8190A-12G	12GSa/s with 12 bit resolution	2		
M8190A-AMP	Additional AC and DC Amplifier	2		
M8190A-SEQ	Sequencer	2		
M8195A-810	Matched Cable Pair for M8195A AWG 2.92 mm	2		
M8070A-OTP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1		
M8070A-ONP	System Software for M8000 Series of BER Test Solutions, Network License	0		
M8070A-1TP	Device Control Interface	1		
M8085CE1A-1TP	MIPI C-PHY 1.2 Editor for M819xA AWG, Transportable, Perpetual License	1		
M8085CC1A-1TP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1		
M8085CE1A-1NP	MIPI C-PHY 1.2 Editor for M819xA AWG, Network/Floating, Perpetual License	0		
M8085CC1A-1NP	MIPI C-PHY 1.2 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	0		
N5990A-010	Bitifye Test sequencer for M8085A C-PHY Products	1		

Ordering a MIPI D-PHY RX Test Configuration

Complete n-Lane D-PHY Setup (HS, LP, and transitions, full compliance) using M8195A modules		1	2	4
Number of D-PHY lanes				
Option	Description	Quantity		
M8195A-BU1	AXIe Chassis: 5-slot with Integrated System Module plus Embedded Controller: Quad Core, 8GB RAM, 160 SSD, 2 GB/s	1	1	1
M8195A-004	Arbitrary Waveform Generator, 4 Channels, 65 GSa/s	1	1	2
M8195A-002	Arbitrary Waveform Generator, 2 Channels, 65 GSa/s	0	1	1
M8195A-001	Arbitrary Waveform Generator, 1 Channel, 65 GSa/s	0	0	0
M8195A-16G	Upgrade to 16 GSa Memory	1	2	3
M8195A-SEQ	Sequencer	1	2	3
M8197A	AWG synchronisation module	0	1	1
M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	1	1
M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0	0	0
M8070A-1TP	Device Control Interface	1	1	1
M8195A-810	Matched Cable Pair for M8195A AWG, 2.92 mm	0	0	0
M8085DE1A-1TP	MIPI D-PHY 2.0 Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085DC1A-1TP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	1	1
M8085DE1A-1NP	MIPI D-PHY 2.0 Editor for M819xA AWG, Network/Floating, Perpetual License	0	0	0
M8085DC1A-1NP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	0	0	0
N5990A-010	Bitfeye Test sequencer for M8085A D-PHY Products	1	1	1
Complete 1-Lane D-PHY Setup (HS, LP, and transitions, full compliance) using M8190A modules		Quantity		
M8190A-BU1	Bundle 1 consisting of M9505A AXIe Chassis w/ 5 slots and M9536A Embedded PC Controller	1		
M8190A-001	Arbitrary Waveform Generator 1 Channel	0		
M8190A-002	Arbitrary Waveform Generator 2 Channel	2		
M8190A-02G	Upgrade from 128Msa to 2GSa Memory/Channel	4		
M8190A-12G	12GSa/s with 12 bit resolution	2		
M8190A-14B	14 Bit resolution at 8GSa/s	0		
M8190A-AMP	Additional AC and DC Amplifier	2		
M8190A-SEQ	Sequencer	2		
M8195A-810	Matched Cable Pair for M8195A AWG 2.92mm	2		
M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1		
M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0		
M8070A-1TP	Device Control Interface	1		
M8085DE1A-1TP	MIPI D-PHY 2.0 Editor for M819xA AWG, Transportable, Perpetual License	1		
M8085DC1A-1TP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Transportable, Perpetual License	1		
M8085DE1A-1NP	MIPI D-PHY 2.0 Editor for M819xA AWG, Network/Floating, Perpetual License	0		
M8085DC1A-1NP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	0		
N5990A-010	Bitfeye Test sequencer for M8085A D-PHY Products	1		



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Keysight Services can help from acquisition to renewal across your instrument's lifecycle. Our comprehensive service offerings—one-stop calibration, repair, asset management, technology refresh, consulting, training and more—helps you improve product quality and lower costs.

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Up to ten years of protection and no budgetary surprises to ensure your instruments are operating to specification, so you can rely on accurate measurements.

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