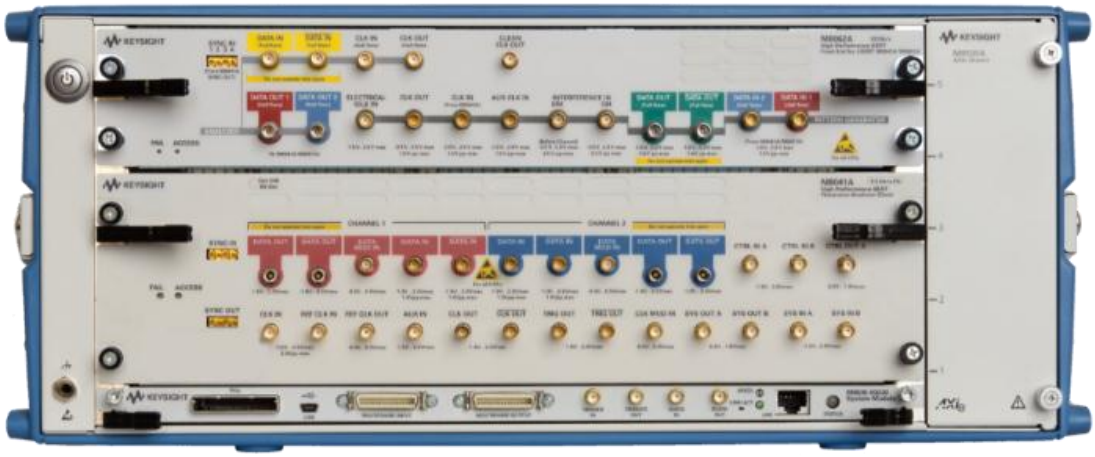
Keysight Technologies

M8062A 32 Gb/s Front-end for J-BERT M8020A High-Performance BERT

Datasheet

Preliminary Version



J-BERT M8020A High-Performance BERT with M8062A and M8041A module

KEYSIGHT TECHNOLOGIES

Key features

- Extends maximum data rate of J-BERT M8020A up to 32.4 Gb/s
- Control of pattern generator and error analyzer seamlessly
- Integrated 8-tap de-emphasis
- Build in ISI generator for channel emulation
- Analyzer equalization eliminates errors resulting from closed eyes in loop back path

Description

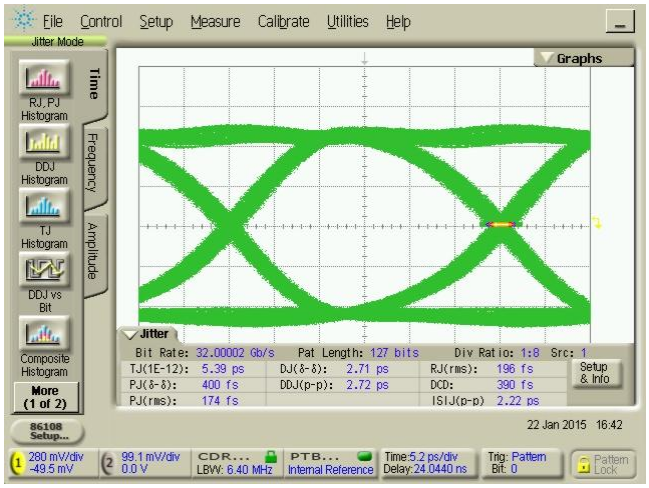
The M8062A extends the data rate of the J-BERT M8020A Bit Error Ratio Tester to the speeds required for testing devices with lane rates in the 25-28 Gb/s range. When combined with a two channel M8041A, the system provides data pattern generation and full rate error analysis for users developing 100G class serial data link components and systems with lane rates up to 32.4 Gb/s.

Typical Applications:

- 100G Serdes development (CAUI-4)
- Optical Transceiver development for 100G-SR4, LR4, and ER4, 32G Fibre Channel
- Thunderbolt 20G
- Active Optical Cables

Characterization and Compliance testing 100G class devices and systems

With a top data rate of up to 32.4 Gb/s, the M8062A with the J-BERT M8020A has the speed required to address 100G class serial links used in data center networking applications, as well as emerging higher speed computer bus standards such as Thunderbolt 20G. In addition to supporting all of the stress types required for compliance testing to these standards, the system offers several features that greatly improve efficiency and accuracy when performing characterization tests.



Eye diagram showing < 200 fs intrinsic jitter

Integrated “tuneable” Inter-Symbol Interference

Most receivers designed for 100G class applications contain equalization to counter the effects of channel loss. The equalization design may be a multi-step CTLE, or a combination of CTLE and DFE Many devices include auto-optimizers which select the optimum equalization settings during a training cycle. To verify the design, the receiver must be tested with a variety of channels to create various amounts of eye closure. Because these designs have multiple CTLE gain, or DFE tap settings, design verification requires inclusion of channel losses in the middle of the operating range, rather than just the minimum and maximum.

Traditionally, testing with a variety of channel losses was a tedious process, requiring changing cables between connectors on test trace boards which emulate various channel lengths. Using this method, the resolution in channel loss is limited. The potential for an auto-optimizing design to fail to converge at a particular intermediate channel loss may not be discovered during characterization testing, if the particular loss which causes the problem lies between the fixed lengths of test channels being used.

The 32G M8020A overcomes both of these problems by offering an electronically tunable ISI generator, for emulating channels. This system adds an electronic filter in the pattern generator data stream. The user can set one or two frequency breakpoints, and select the loss value at each, providing continuously adjustable frequency dependent loss to emulate virtually any channel loss.

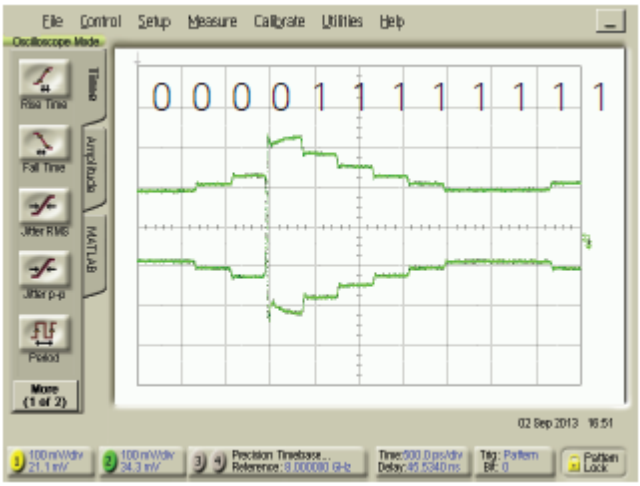
Adjust loss and import of S21 parameters, preliminary M8070A screen shot

In addition to direct control through the user interface built into the M8070A BERT control software, the loss parameters can be set through remote programming commands, allowing test automation. By eliminating the need to manually move cables, cauterization testing of receiver equalization becomes much more efficient.

Emulate transmitter de-emphasis with high precision

Virtually all transmitters for 100G class links include multi-tap de-emphasis. The 32G J-BERT M8020A system offers integrated 8 tap de-emphasis, to emulate the system transmitter, or simply de-embed the cables and test fixtures from the test set-up.

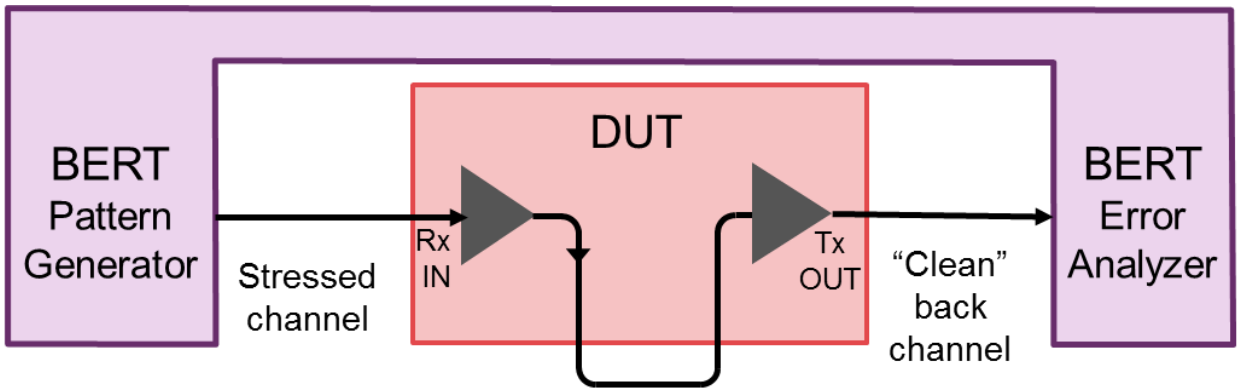
Up to 8 taps can be configured as 5 post cursor, and two pre-cursor. Tap weights are individually settable, with essentially no interaction.



De-emphasis capability is built into the M8062A, not requiring external “signal processing boxes” which add cables and complicate the test set-up.

Integrated analyzer equalization

In a traditional receiver test setup, the receiver under test is fed a stressed test pattern from the pattern generator, and the received signal is looped back and re-transmitted to the BERT error analyzer. The loopback channel is not "stressed" to preserve the eye quality for accurate BER measurements

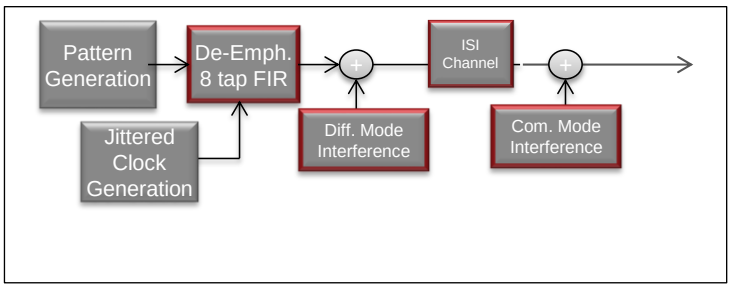


At 25-28 Gb/s, even the "clean low loss" back channel which feeds the BERT error analyzer will have some loss and eye closure. Jitter in the retransmitted receiver data can introduce errors at the input of the error analyzer when the eye is closed excessively, resulting in overstated bit errors.

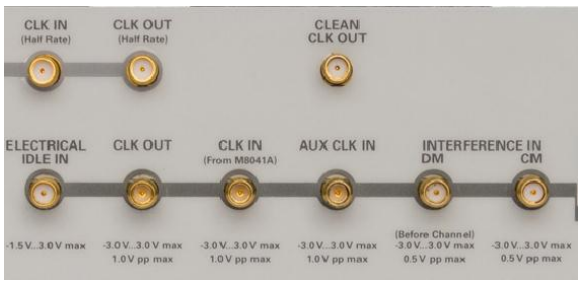
Adding equalization to the input of the error analyzer opens partially closed eyes in the back channel, minimizing the possibility of errors in the BER measurement

Integrated Interference Injection

The M8062A provides the same inputs for interference injection (amplitude noise) as in the 16G BERT. Connectors allow introduction of interference sources such as sine wave generators or random noise sources directly into the pattern generator data. Both Common Mode and Differential Mode injection paths are provided. The Common Mode is added at the end of the ISI channel, whereas the Differential Mode is injected before – as directed by many of the computer bus standards which require interference injection as part of the receiver test stress recipe.



Blockdiagram pattern generator & distortion sources



Input connectors for level interference (on the right side)

Specification

Pattern Generator Data out	Target Specification
Output data rate	512 Mb/s to 32.4 Gb/s
Channels	1
Data format	Non-Return to Zero (NRZ), single ended and differential
Output amplitude	0.05 Vpp to 1.2 Vpp (single ended) 0.1 to 2.4 Vpp (differential) See next table for max output amplitude if offset is > 1.9V and CM1 / DM1 are turned on
Output resolution	1 mV (single-ended)
Voltage window	-1 V to +3 V
External termination voltage	-1 V to + 3V For offset > 1.3V the termination voltage should be +/- 0.5V offset
Transition times	12 ps typical (20/80) [1]
Intrinsic random jitter	< 200 fs rms typical, >25 Gb/s, using internal clock
Total jitter	6 ps pp typical @ PRBS $2^{15} - 1$, at a target BER of 10^{-12}, room temperature [2,3]
Peak-peak jitter	6 ps pp typical @ PRBS $2^{31} - 1$, based on 1000 waveforms captured at 50 % crossing point[2,3]
Adjustable Inter-symbol Interference (ISI)	Yes, details tbd
Crossing point	Adjustable form 30 % to 70 % typical
Electrical idle transition time	Output transitions from full swing signal to 0 V amplitude and vice versa at constant offset within 4 ns typical. Latency is TBD.
Jitter pass through	All jitter sources in the M8041A pass through the M8086A transparently except F/2 jitter
Variable clock/2 jitter injection	up to ±0.1 UI or ±20 ps (whatever is less)
Output protection	This is an emergency shutdown feature. It disables an output in case an unexpected voltage is detected. DC coupling mode: Termination range for devices connected to data out: unbalanced 50 Ω ± 10 Ω typical balanced 100 Ω ± 20 Ω typical Operation into open is possible for these ranges when "DC coupled" and "balanced" termination modes are selected: output amplitude max. 300 mV [4] offset 0 to 270 mV AC coupling mode: An external DC blocking capacitor is expected. If a resistive load is discovered the output will not be enabled.
Connectors	2.4 mm female
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage.

1. Measured with DCA-X 86118A.
2. Measured with Oscilloscope with < 50 fs rms intrinsic jitter, such as 86108B with HBW and PTB.
3. Measured at a data rate of 28.4 Gb/s, using the Keysight E8257D-520 as precision clock source.
4. Per output when differentially terminated into 100 Ω. Results in doubled swing when driving into open.

Data output amplitude maximum in presence of CMI, DMI, offset voltage

CMI	DMI	Offset ≤1.9 V	Offset > 1.9 V
Disabled	Disabled	1.2 V	0.9 V
Disabled	Enabled	0.9 V	0.675 V
Enabled	Disabled	0.9 V	0.75 V
Enabled	Enabled	0.675 V	0.5625 V
Enabled	Enabled (1)	0.8 V	0.666

(1) For DMI < 12.5 % of amplitude

De-emphasis of data out (option 0G4)	Target Specification
De-emphasis taps	8
Pre-cursor 2	±6.0 dB
Pre-cursor 1	±12.0 dB
Post-cursor 1	±20.0 dB
Post-cursor 2	±12 dB
Post-cursor 3	±6 dB
Post-cursor 4	±6 dB
Post-cursor 5	±6 dB
De-emphasis tap resolution	0.1 dB

Footnote: Sum of all cursors may not exceed Vpp max

Pattern Generator Clocks (Half Rate)	Target specification
Frequency range	256 MHz to 16.2 GHz
Clock out amplitude	1 Vpp typical, single ended
Clock out interface	AC coupled, 50 Ω nominal
Aux clock input	For alternate clock input
Aux clock input amplitude	0.2 to 1.0 V
Aux clock input transition time	< 200 ps
Clean clock out amplitude	1 Vpp typical
Clean clock out divide ratios	1, … N, from 256-16 GHz 2, … N, even only, from 16-16.2 GHz N is limited such that the minimum clock frequency is ≥ 2 MHz
Clean clock out interface	AC coupled, 50 Ω nominal
Clock connectors	3.5 mm female

CMI/DMI In, Electrical Idle In	Target Specification
Input voltage (CMI, DMI)	400 mV single ended, nominal
Common mode interference (CMI) input (external source needed)	0 to 400 mV, corresponds to gain range 0 to 1 10 MHz to 1 GHz
Differential mode interference (DMI) input (external Source needed)	0 to 30% of output amplitude, corresponds to gain range 0 to 1 10 MHz to 6 GHz
EIDL input threshold voltage	-1 to +3 V
EIDL input termination voltage	-1 to +3 V
EIDL connector	SMA connector

Analyzer Data In	Target Specification
Data rate	512 Mb/s to 32.4 Gb/s
Channels	1
Data format	NRZ, single ended and differential
Input sensitivity	50 mV, min. differential
Max swing	1.6 Vpp differential
Input interface	100 Ω differential, 50 Ω single ended, AC coupled
Clock-to-data delay timing resolution	tbd
Input connectors	2.4 mm, female

Analyzer Equalizer	Target Specification
Equalization	Allows recovery of data from partially closed eyes for BER measurement.
Gain range	9 dB at 16 GHz
Equalization settings	Low, ≈3 dB Med, ≈6 dB High, ≈9 dB, nominal (0 dB)
Analyzer Clock In (half rate)	**Target Specification**
Frequency range	256 MHz to 16.2 GHz
Input voltage amplitude range	0.3 to 1.0 Vpp
Input clock transition time	tbd
Interface	AC coupled, 50 Ω, nominal
Connector	3.5 mm, female

User interface and remote control interface	
BERT software	M8070A
External controller	PCIe connectivity: Please refer to list of tested PCs in the technical note: 5990-7632EN USB connectivity,
Connectivity AXIe chassis	USB 2.0, PCIe 2.0 / 8x
Programming interface	SCPI

Product options	
Options are field upgradeable except for -0A4	
M8062A-C32	32 Gb/s BERT front-end
M8062A-G32	32 Gb/s Pattern generator front-end
M8062A-0G4	8-tap de-emphasis license
M8062A-0G5	Adjustable interference license
M8062A-0A4	Clock recovery up to 32 Gb/s (1)
M8062A-0A3	Analyzer equalization license

(1) M8062A-0A4 will be shipped with the 2nd release. Requires return to factory recalibration for 1st release instruments

General characteristics	
Operating temperature	5 – 40 C
Storage temperature	-40 to 70 C (module)
Operating humidity	15% to 95% relative humidity at 40 C (non-condensing)
Storage humidity	24 % to 90% relative humidity at 65 C (non-condensing)
Power requirements (module only)	tbd
Physical dimension (W x H x D)	Module in a 5-slot AXIe chassis 143 x 194 x 446 mm
Weight	Module:4.1 kg (9.0 lb)
Recommended recalibration period	1 year

myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

Three-Year Warranty
www.keysight.com/find/ThreeYearWarranty
Keysight's commitment to superior product quality and lower total cost of ownership. The only test and measurement company with three-year warranty standard on all instruments, worldwide.

Keysight Assurance Plans
www.keysight.com/find/AssurancePlans
Up to five years of protection and no budgetary surprises to ensure your instruments are operating to specification so you can rely on accurate measurements.

www.keysight.com/go/quality
Keysight Technologies, Inc.
DEKRA Certified ISO 9001:2008
Quality Management System

Keysight Channel Partners
www.keysight.com/find/channelpartners
Get the best of both worlds: Keysight's measurement expertise and product breadth, combined with channel partner convenience.

www.keysight.com/find/M8062A

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
www.keysight.com/find/contactus

Americas

Canada	(877) 894 4414
Brazil	55 11 3351 7010
Mexico	001 800 254 2440
United States	(800) 829 4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 6375 8100

Europe & Middle East

Austria	0800 001122
Belgium	0800 58580
Finland	0800 523252
France	0805 980333
Germany	0800 6270999
Ireland	1800 832700
Israel	1 809 343051
Italy	800 599100
Luxembourg	+32 800 58580
Netherlands	0800 0233200
Russia	8800 5009286
Spain	800 000154
Sweden	0200 882255
Switzerland	0800 805353 Opt. 1 (DE) Opt. 2 (FR) Opt. 3 (IT)
United Kingdom	0800 0260637

For other unlisted countries:
www.keysight.com/find/contactus

Published in USA, March 27th 2015
www.keysight.com