Agilent M8061A 28 Gb/s Multiplexer with De-Emphasis

Data Sheet Version 1.1

Key features

- Expands data rate of J-BERT N4903B pattern generator up to 28.4 Gb/s
- Integrated and calibrated 4-tap de-emphasis, expandable to 8 taps
- Internal superposition of interference for common-mode and differential mode
- Transparent to jitter generated by J-BERT, Clock/2 jitter can be added
- Electrical idle
- Control from J-BERT N4903B user interface via USB

Description

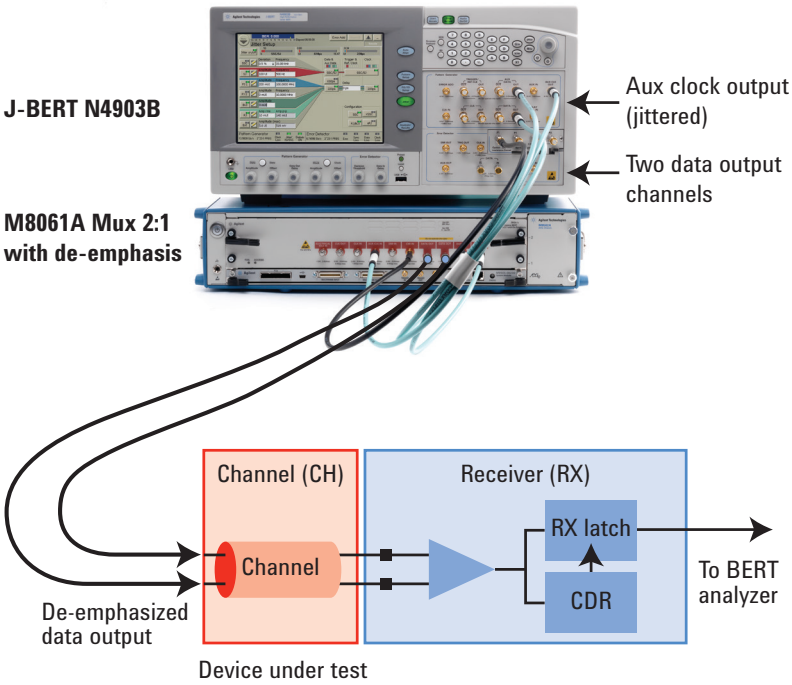
The R&D and test engineers who need to characterize serial interfaces of up to 28.4 Gb/s can use the M8061A 2:1 Multiplexer with optional de-emphasis to extend the rate of J-BERT N4903B pattern generator. For the most accurate receiver characterization results, the M8061A provides four calibrated de-emphasis taps, which can be extended to eight taps, built-in superposition of level interference and Clock/2 jitter injection. The M8061A is a 2-slot AXIe module that can be controlled via USB from J-BERT's user interface.

Data rates up to 28.4 Gb/s are used for testing:

- Optical transceivers such as 100GBASE-LR4, -SR4 and -ER4, 32G Fibre Channel
- SERDES and chip-to-chip interfaces, such as OIF CEI
- Backplanes, cables, repeaters, such as 100GBASE-KR4, -CR4
- Next generation computer buses, such as PCIe4

Emulate transmitter de-emphasis with up to 8 taps

Many multi gigabit serial interfaces use transmitter de-emphasis to compensate for electrical signal degradations caused by printed circuit boards or cables between the transmitter and the receiver ports. R&D and test engineers who need to characterize receiver ports under realistic and worst case conditions require a pattern generator that allows to accurately emulate transmitter de-emphasis with adjustable multi-tap de-emphasis levels. The M8061A can be used in combination with J-BERT N4903B as shown below.



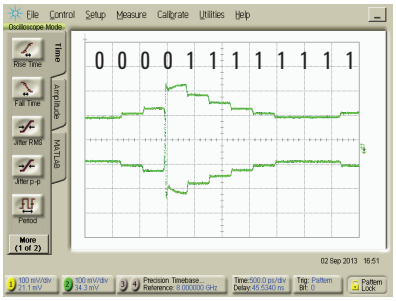


Figure 1. This test setup shows how to emulate transmitter de-emphasis up to 28.4 Gb/s with M8061A and J-BERT N4903B.

De-embed signal degradations caused by the test set up and fixtures using de-emphasis

Minimzing the influence of the test environment is a challenge especially if bit rates exceed 20 Gb/s. To de-embed the signal degradations caused by cables, test fixtures, adapters, etc. The de-emphasis technique is commonly used. M8061A is the only instrument that offers up to 8 tap de-emphasis up to 28.4 Gb/s, allowing compensation of signal degradations in very fine steps.

Emulate channel loss with negative de-emphasis

Channel losses can be emulated by using the negative de-emphasis funcion of the M8061A. See figure 2. The post-cursor taps can be used to emulate channel losses for higher frequencies. As a guideline: with the 5 post-cursor taps of M8061A loss frequencies above f / 5 can be emulated; for example for a data rate of 28 Gb/s, f equals 14 GHz, and f/5 corresponds to 2.8 GHz. See figure 3.

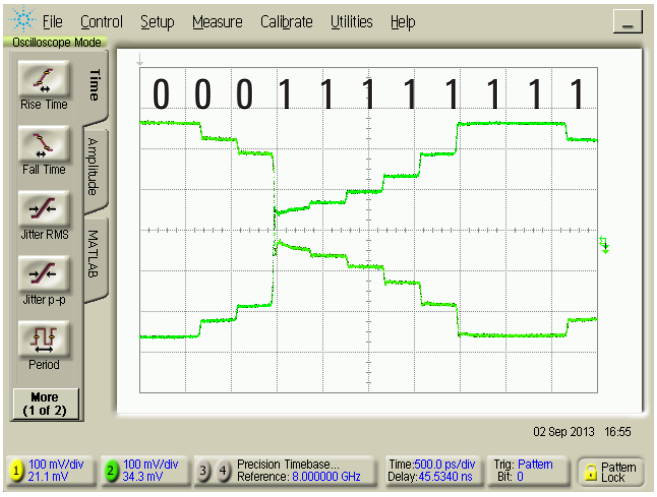


Figure 2. Emulate high-frequency channel losses by using M8061A's with inverted de-emphasis taps. The differential signal shows a pattern of eight 0's and eight 1's. Pre-cursor 2+1: -1.5 dB. Post-cursor 1,2,3,4,5: +1.5 dB.

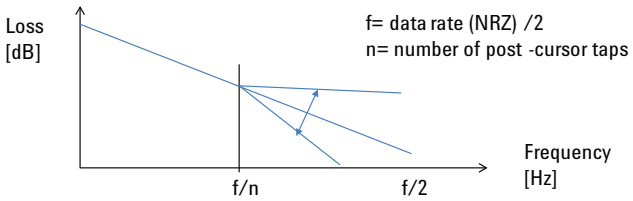


Figure 3. Emulate high-frequency channel losses by using the negative de-emphasis capability of M8061A.

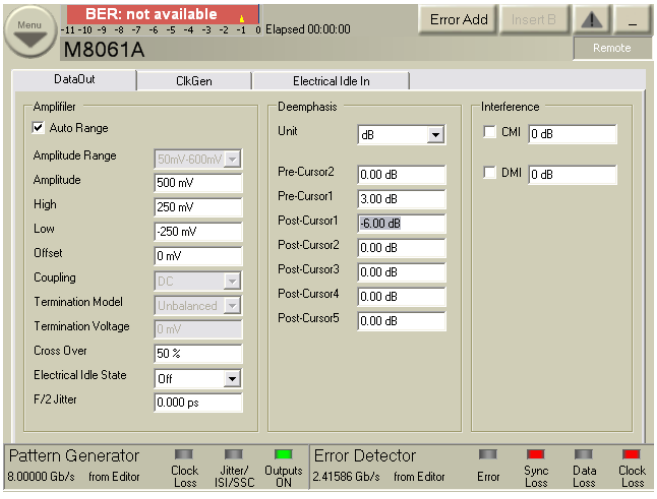


Figure 4. Users can control all M8061A parameters via the J-BERT N4903B GUI and remote control interface. M8061A is connected via USB 2.0 to J-BERT.

Accurately characterize receivers up to 28.4 Gb/s

Many SERDES, backplane, cables and optical receivers operate at data rates of 25 Gb/s and beyond. To characterize the receiver tolerance against jitter, x-talk, level interference, and voltage sensitivity the M8061A can be used as 2:1 multiplexer to extend the data rate of the J-BERT N4903B pattern generator up to 28.4 Gb/s. It can operate with a clean clock source to achieve lowest intrinsic jitter. But it can also be used to provide calibrated jitter, because it is transparent to the calibrated jitter from J-BERT and offers additional Clock/2 jitter injection. Built-in interference superposition (common-mode and differential mode) eliminates the need for external adders.

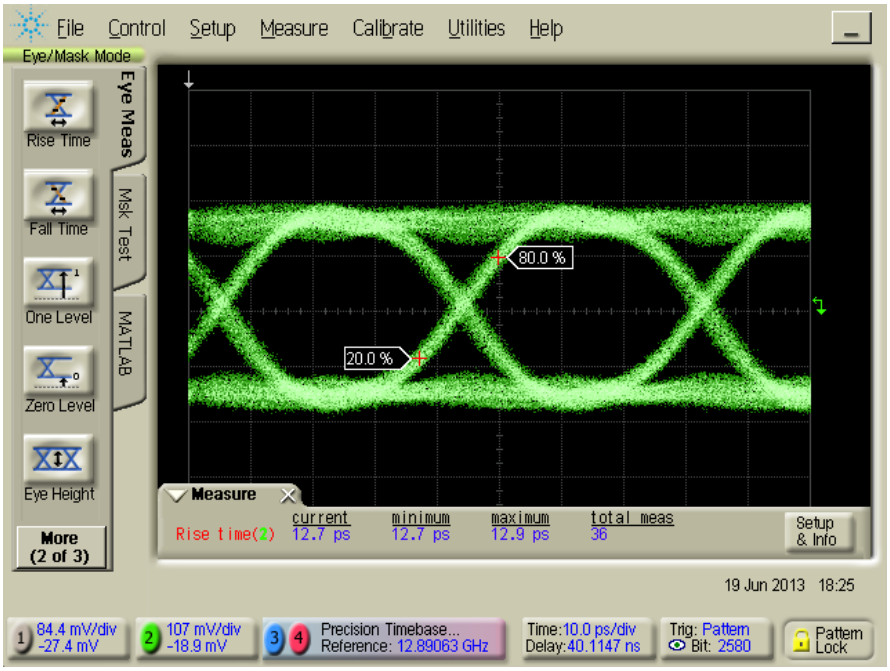


Figure 5. Output signal of M8061A with de-emphasis turned off. Measured with 86118A, clocked from J-BERT with PRBS 2^{15}-1 pattern and 350 mVpp output voltage.

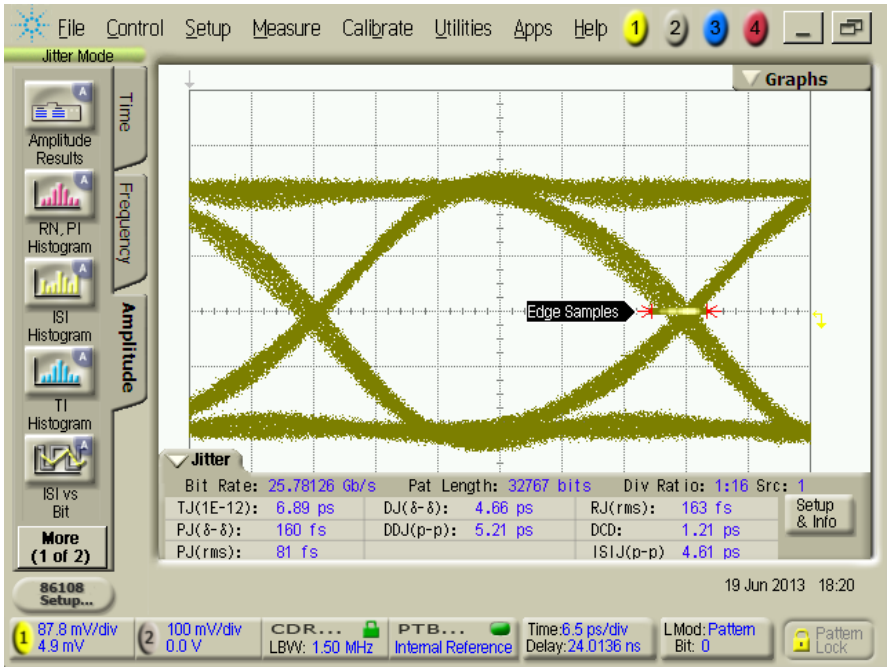


Figure 6. Shows the very low intrinsic random jitter of the M8061A output. The screen shot is taken with Agilent 86108B, a clock pattern, clocked from the precision clock source E8257D.

M8061A specifications

The specifications below apply for use with J-BERT N4903B. When used with J-BERT M8020A the max. data rate is 32.4 Gb/s. See supplementary specifications in M8020A data sheet.

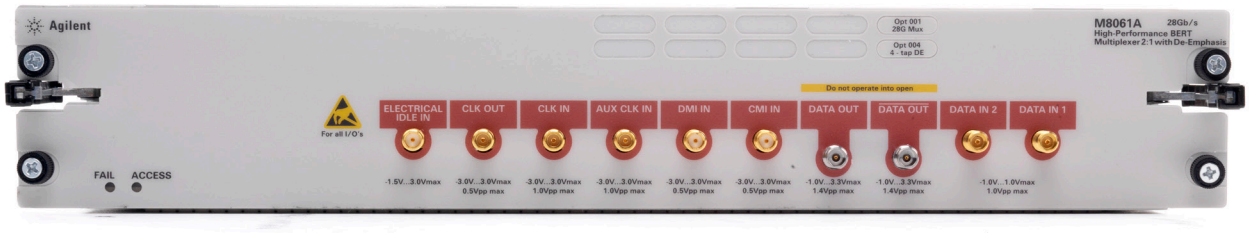


Figure 4. Front panel of M8061A module.

Table 1. Specifications for data out

Output data rate	300 Mb/s to 27.0 Gb/s (28.4 Gb/s when using J-BERT N4903B option D14)
Output format	NRZ
Output amplitude	0.05 Vpp to 1.200 Vpp, 5 mV resolution (for single ended operation) 0.1 to 2.4 Vpp differential. See table 2 for max. output amplitude if offset is > 1.9 V and CMI/DMI are turned on.
Output voltage window	–1 V to +3 V
External termination voltage	–1 V to +3 V For offset > 1.3 V the termination voltage should be ± 0.5 V of offset.
Transition times	14 ps typical (20% to 80%) for data rates > 25 Gb/s, de-emphasis disabled
Intrinsic random jitter [1]	200 fs rms typical with external clock from Precision Signal Generator E8257D-520 and clock pattern. When using J-BERT N4903B as clock source, its intrinsic clock jitter applies.
Total jitter [1, 2]	6 ps pp typical @ PRBS 2^{15} -1, at a target BER of 10^{-12}, room temperature
Peak-peak jitter [1, 2]	6 ps pp typical @ PRBS 2^{31} -1, based on 1000 waveforms captured at 50% crossing point
Jitter feed-through	Transparent for timing jitter on clock. ISI has to be added after multiplexer. *Notice: When controlled from J-BERT the jitter amplitude values refer to the output of M8061A (2 UI)*
Variable clock/2 jitter	± 0.1 UI or ± 20 ps typical (whatever is less) *Notice: This means that first eye can be up to 20 ps longer or shorter than subsequent eye.*
Crossing point	Adjustable 30% to 70% typical
Electrical idle transition time	4 ns typical + 60 ns ± 10 ns (reaction time from EIDLE input to data outputs starting to go into EIDL state)
Interface	Differential or single-ended, DC coupled, 50 Ω output impedance
Connectors	2.4 mm, female

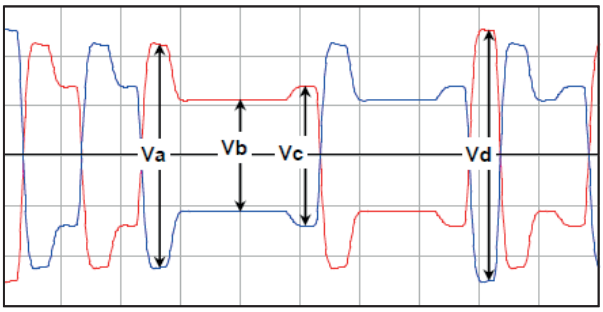
1. *Measured with Oscilloscope with < 50 fs rms intrinsic jitter, such as 86108B with HBW and PTB.*
2. *Measured at a data rate of 28.4 Gb/s, using the Agilent E8257D-520 as precision clock source.*

Table 2. Data output amplitude maximum in presence of CMI, DMI, offset voltage			
CMI	DMI	offset ≤ 1.9 V	offset > 1.9 V
Disabled	Disabled	1.2 V	0.9 V
Disabled	Enabled	0.9 V	0.675 V
Enabled	Disabled	0.9 V	0.75 V
Enabled	Enabled	0.675 V	0.5625 V
Enabled	Enabled [1]	0.8 V	0.666 V

1. For DMI < 12.5% of amplitude.

Table 3. Specifications for de-emphasis at data out (Option 004 and 008)		
	Option 004 (4 taps)	Option 008 (extension to 8 taps)
Pre-cursor 2 range		± 6 dB
Pre-cursor 1 range	± 12 dB	
Post-cursor 1 range	± 20 dB	
Post-cursor 2 range	± 12 dB	
Post-cursor 3 range		± 12 dB
Post-cursor 4 range		± 6 dB
Post-cursor 5 range		± 6 dB
Cursor accuracy	± 1.0 dB typical at 8 Gb/s at PCIe 3 presets	n/a
Cursor resolution	0.1 dB	0.1 dB

Footnote: Sum of all cursors may not exceed Vpp max.



Post-cursor 1 = $20\log_{10}$ Vb/Va
Pre-cursor = $20\log_{10}$ Vc/Vb
Vpp nominal = $20\log_{10}$ Vd

Figure 5. Definition of nominal output amplitude and de-emphasis (aligned to N4916B and PCI-SIG PCI Express 3.0 specification).

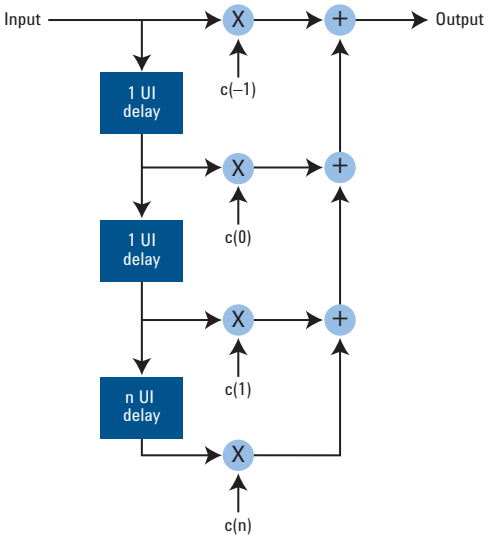


Figure 6. Simplified block diagram for multi-tap FIR (finite pulse respone) circuit.

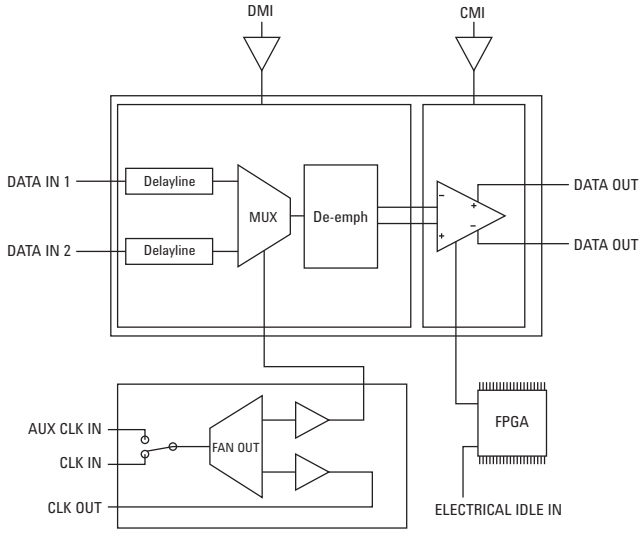


Figure 7. Blockdiagram of M8061A.

Table 4. Specifications for data in	
Input voltage data inputs	500 to 800 mVpp single ended and -70 mV offset (this is automatically set when controlled from J-BERT N4903B)
Input format	NRZ
Interface	Single-ended, 50 Ω input impedance
Connectors	3.5 mm, female

Table 5. Specifications for clock out, aux clock in and clock in	
Frequency range	150 MHz to 14.2 GHz
Input format	RZ, full rate
Input voltage clock inputs	0.2 to 1.0 V
Input clock transition time	< 200 ps
Amplitude clock output	1 Vpp typical, single ended
Interface	AC coupled, 50 Ω nominal
Connector	3.5 mm, female
CLK IN	For clean clock input from PSG
AUX CLK IN	For jittered clock from N4903B AUX CLK output

Table 6. Specifications for CMI in, DMI in, electrical idle in		
	Differential mode interference (DMI)	Common mode interference (CMI)
Input voltage	Nominal: 400 mV single ended	
Modulation bandwidth	10 MHz to 6 GHz	10 MHz to 1 GHz
Modulation amplitude	0% to 30% of output amplitude	0 to 400 mV
	corresponds to gain range of 0 to 1	
EIDL input threshold voltage range	–1 to +3 V	
EIDL input termination voltage	–1 to +3 V	
Connectors	SMA	

Table 7. General characteristics	
Operating temperature	5 °C to 35 °C (–23 to + 95 °F)
Storage temperature	–40 °C to +70 °C (module) (–65 to + 158 °F)
Operating humidity	15% to 95% relative humidity at 35 °C (non-condensing)
Storage humidity	90% to 24% relative humidity at 65 °C (non-condensing)
Power requirements	90 VA
Physical dimensions (W x H x D)	**2-slot AXIe module:** 351 x 61 x 315 mm (13.8 x 2.4 x 12.4 in) **Installed in 2-slot AXIe chassis:** 463 x 105 x 428 mm (18.2 x 4.1 x 16.9 in)
Weight net	**Module:** 4.1 kg (9.0 lb) **Installed in 2-slot-AXIe chassis:** 11.8 kg (26.0 lb)
Weight shipping	**Module:** 7.1 kg (15.7 lb) **Installed in 2-slot-AXIe chassis:** > 38 kg (> 83.8 lb), palletized
Recommended recalibration period	1 year
Warranty period	3 years return to Agilent
Warm-up time	30 minutes
Cooling requirements	Slot airflow direction is from right to left. To ensure adequate cooling and ventilation, leave a gap of at least 50 mm (2 ") around vent holes on both sides of the chassis. See also Start-up guide for M9502A chassis.
EMC	IEC 61326-1
Safety	IEC 61010-1
Quality management	ISO 9004, 14001

Table 8. Remote control interface	
Interface to controlling J-BERT	USB 2.0 mini (requires AXIe chassis with USB option, e.g. M9502A-U20 or M9505A-U20)
Programming language	SCPI
Via J-BERT N4903B	Via USB, requires N4903B SW rev 7.50 or later
Download latest software	For J-BERT N4903B: ***www.agilent.com/find/n4903***

Specification assumptions

The specifications in this document describe the instruments warranted performance when used with J-BERT N4903B. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All specifications if not otherwise stated are valid using the recommended cable set N4910A (2.4 mm, 24" matched pair).

Related Agilent literature

J-BERT N4903B High-Performance Serial BERT - Data Sheet	5990-3217EN
J-BERT M8020A High-Performance BERT - Data Sheet	5991-3647EN
N4877A Clock Data Recovery and Demultiplexer 1:2, N1075A Optical Pick-Off/Converter, N1070A Optical Clock Recovery Solution, Data Sheet	5990-9949EN
Error Detection Up to 28.4 Gb/s During Receiver Test with the Agilent J-BERT N4903B Using Under-Sampling Techniques, Application Note	5990-6239EN
M9502A and M9505A 2- and 5-Slot AXIe Chassis, Data Sheet	5990-6584EN
2-Slot and 5-Slot AXIe Chassis M9502A, M9505A, Start-up Guide	M9502-90001

Ordering instructions

The M8061A module includes the following accessories by default: Two 50 Ω terminations, USB cable, getting started guide, commercial calibration report ("UK6"), ESD protection kit. For M8061A-BU2 some additional accessories for the AXIe chassis are provided, such as getting started guide, filler panel.

Multiplexer 2:1 up to 28.4 Gb/s	M8061A-001
De-emphasis, 4 calibrated taps	M8061A-004
De-emphasis, extension to 8 taps	M8061A-008
Bundle consisting of M9502A-U20 AXIe 2 slot chassis with USB option	M8061A-BU2
Matched cable kit for connecting M8061A with J-BERT N4903B (required)	M8061A-801
Recommended accessories	
Matched cable pair, 2.4 mm (f) to 2.4 mm (f)	N4910A
Four SMA cables, unmatched	15442A
2.92 mm (f) - (f) matched cable pair, 50 Ω, 0.85 m (recommended for data signal connection with M8020A and with N4877A)	M8041A-801
SMA cable, 50 Ω, 0.46 m (recommended for clock signal connection with M8020A)	M8090A-810
6 dB attenuator, 50 GHz (when data outputs is driving into non- 50 Ω inputs and for over-voltage protection, e.g. for some high-performance oscilloscopes)	8490D
DC block, 50 GHz (when data output drives into a single ended, AC coupled input, such as 81490A ref. transmitter)	9398F
Rack-mount kit for AXIe 2-slot chassis M9502A	Y1225A
5-slot AXIe chassis (alternatively to M8061A-BU2) with USB option	M9505A-U20
External USB hub 6:1 with power supply	non-Agilent
Warranty, calibration and productivity services	
Extended 5 year warranty Return-to-Agilent	R1280
Calibration services (3 and 5 years)	R1282
Productivity assistance	R1380-N49xx
Recommended J-BERT N4903B configuration	
N4903B with options -C13, -002, and -D14. Optional: N4903B -J10 (jitter sources), -J20 (interference and ISI). Optional: E8257D-520 (Precision Signal Generator 20 GHz as clean clock source) Optional: N4877A-232 clock data recovery and de-multiplexer	

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