M8040A High-Performance BERT 64 Gbaud

Version 3.0

Master your next design

New features:
- – Integrated clock recovery
- – PCI Express 5.0® support
- – ISI channel boards
- – Error distribution analysis

KEYSIGHT
TECHNOLOGIES

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Introduction

The Keysight Technologies Inc. M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level (PAM4) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 Gbaud (corresponds to 128 Gbit/s) can be used for testing devices designed for 400/ 200 GbE, OIF CEI-56G and CEI-112G, PCIe® 32/16/8 GT/s, Thunderbolt 3.

The M8040A BERT´s true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

Key features

- Data rates from 2 to 32 and 64 Gbaud
- PAM4 and NRZ selectable from user interface
- Built-in 5 tap de-emphasis to compensate loss
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, and clk/2 jitter
- Forward Error Correction (FEC) encoding and error insertion for testing DUTs with FEC decoder
- Two pattern generator channels per module to emulate aggressor lane
- Linearity tests with adjustable PAM4 levels
- Interactive link training and SKP OS filtering for 8/16/32 GT/s PCI Express®
- Short connections to the DUT with remote heads for the pattern generator
- True PAM4 error detection in real-time for low BER levels
- Built-in and adjustable equalization to re-open closed eyes
- Integrated clock recovery and control of external clock recovery units N1076A/B, N1077A, N1078A
- RI and SI level interference injection via M8054A interference source or M8195A/96A AWG
- Graphical user interface and remote control via M8000 system software
- Error distribution analysis to debug bursted error conditions
- Scalable and upgradeable with options and modules

Applications

The M8040A is designed for R&D and test engineers who characterize chips, devices, transceiver modules and sub-components, boards and systems with serial I/O ports operating with symbol rates up to 32 Gbaud and 64 Gbaud in the data center, computer, server and communications industries.

The M8040A can be used for receiver (input) testing for many emerging interconnect standards, such as:
- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- OIF CEI - 56G (NRZ and PAM4 versions)
- PCI Express 32/16/8 GT/s
- Thunderbolt 3
- 64G/112G Fibre Channel
- Infiniband-HDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

M8000 Series of BER Test Solutions

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

New: PAM4 BERT
up to 64 Gbaud

Figure 1. The M8000 Series BER test solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

The M8040A high-performance BERT 64 Gbaud extends the M8000 Series for 400G data center interconnect testing and PCIe 5 and TBT 3 receiver characterization.

M8040A High-performance BERT 64 Gbaud

Simplifies accurate receiver characterization of devices operating up to 32 and 64 Gbaud with NRZ and PAM4 signals

Highest level of integration streamlines receiver test setups

With the M8040A, all critical test capabilities for input/receiver (RX) characterization are built-in. The pattern generator module provides calibrated and integrated jitter sources and de-emphasis to emulate the transmitter (TX) and to compensate for channel loss in the test setup. In addition, the M8040A provides an internal clock synthesizer and a second pattern generator output channel to emulate an aggressor lane.

The analyzer provides true PAM4 and NRZ error analysis in real time and full sampling to measure down to very low BER and SER.

This high level of integration with the M8040A makes the receiver test set-up connections easier and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of re-adjustments is reduced, resulting in a more efficient use of overall test time.

Loopback to error analyzer

DUT

PAM4 and NRZ
1 and 2 channel pattern generator
with remote heads, de-emphasis and

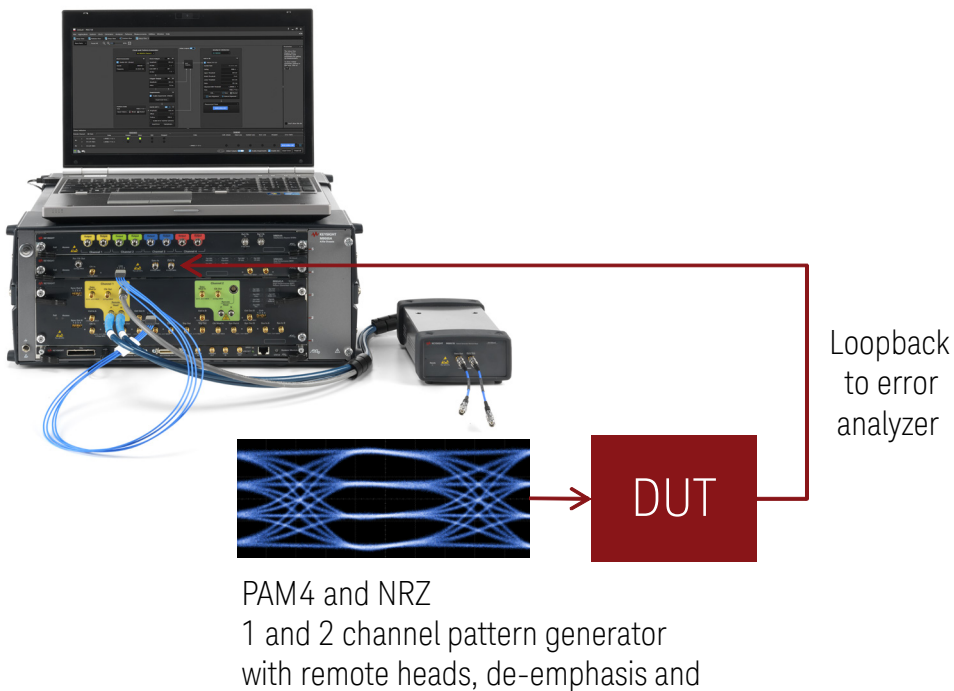Figure 2. The M8040A streamlines complex receiver test setups. Each of the 1 or 2 pattern generator channels provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real-time for NRZ and PAM4 signals without the need to split up the PAM4 signal for multiple error detector channels.

Repeatable and Accurate Results with M8040A

The M8040A high-performance BERT provides clean NRZ and PAM4 signals up to 64 Gbaud with fast transitions and low intrinsic jitter. The remote head concept of M8040A with the short 1.85 mm cables brings the performance close to the device under test, minimizing signal degradations caused by lossy channels.

Figure 3. The remote head M8057A is required for each channel and is required for NRZ and PAM4 signals. It contains an adjustable gain amplifier without re-timer. Users can select NRZ or PAM4 coding and de-emphasis taps settings from the user interface with no need to reconnect cables. The cable between the remote head and the module is 0.85 m long. This allows positioning the remote head closely to the test board for the device under test.

Figure 5. Clean 58 Gbaud NRZ output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2^{15}-1. Measured with Infiniium DCA-X 86100D.

Figure 4. Clean 30 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2^{15}-1. Measured with Infiniium DCA-X 86100D.
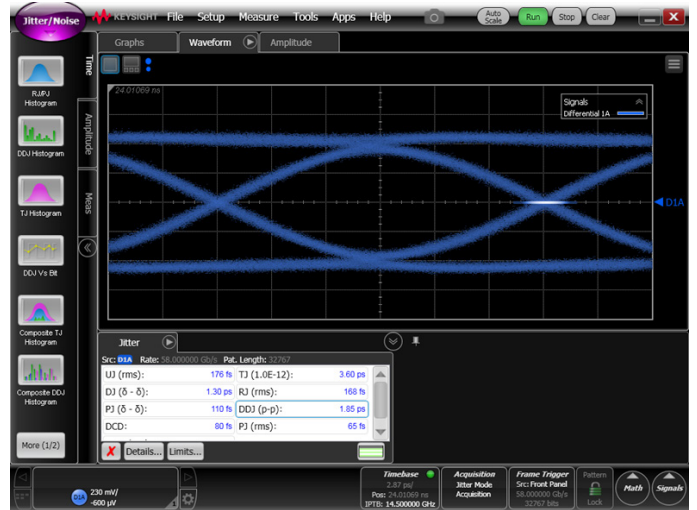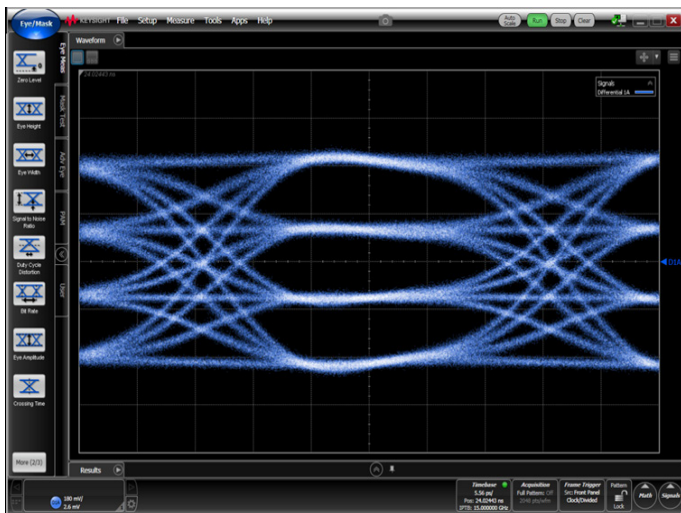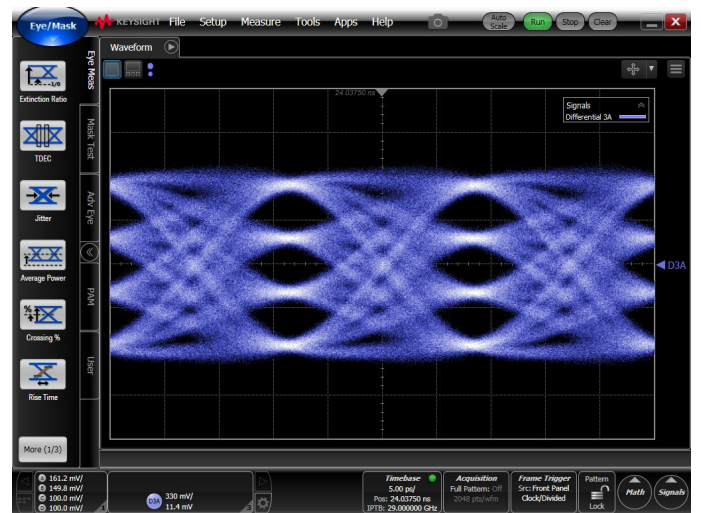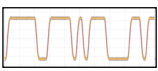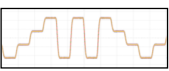

Figure 6. Clean 58 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2^{15}-1.

Emulate Stress Conditions for NRZ and PAM4 Input Tolerance Testing with M8040A

M8040A provides all capabilities required for input tolerance test:

– 1 or 2 channels. Second channel can be used as aggressor lane to emulate crosstalk effects
– Data rates are adjustable from 2 Gb/s NRZ up to 64 Gbaud PAM4, selectable NRZ or PAM4
– Algorithmic PRBS, QPRBS and memory-based patterns, pattern sequencer with loops, error injection
– Generates FEC encoded patterns with pre-coder on 1 lane to test DUTs with FEC decoder
– Built-in and calibrated jitter sources that can be used simultaneously: RJ, multi-UI low-frequency jitter, multi-tone high-frequency jitter, BUJ, clk/2 jitter, spread-spectrum clocking (SSC)
– De-emphasis for pre- and post-cursor to emulate transmitter de-emphasis and compensate for loss in the test setup
– Inject random interference (RI) and sinusoidal interference (SI) by couplers. The M8000 software controls M8054A, AWG M8195A and M8196A as RI/SI source or as aggressor lanes
– Automated jitter tolerance testing

	NRZ	PAM4
Effective data rate	Bit rate	Symbol rate
32 Gbit/s	32 Gb/s	16 GBaud
64 Gbit/s	64 Gb/s	32 GBaud
128 Gbit/s	128 Gb/s	64 GBaud

Covered by M8040A

Related IEEE802.3cd 50/100/200GBASE/GAUI proposed symbol rate * # of lanes	Related IEEE802.3bs 200GBASE/200GAUI symbol rate * # of lanes	Related IEEE802.3bs 400GBASE/400GAUI symbol rate * # of lanes	Related OIF CEI-56G symbol rates	
25. 78125 Gb/s Gb/s NRZ * 1 lane	26.5625 Gbit/s NRZ * 8 lanes	26.5625 Gbit/s NRZ * 16 lanes		
26.5625 Gbaud PAM4 *1/2/4 lanes 53.125 Gbaud PAM4 *1/2 lanes	26.5625 Gbaud PAM4 * 4 lanes	26.5625 Gbaud PAM4 * 8 lanes 53.125 Gbit/s NRZ * 8 lanes	LR-PAM4: MR-PAM4: MR-NRZ: VSR-PAM4: VSR-NRZ: XSR-PAM4: XSR-NRZ: USR-NRZ:	19.6 to 30 Gbaud 18 to 29 Gbaud 39 to 56.2 Gbit/s 18 to 29 Gbaud 39 to 56.2 Gbit/s 18 to 29 Gbaud 39.8 to 58 Gbit/s 19.6 to 58.0 Gbit/s
		53.125 Gbaud PAM4 * 4 lanes		

Figure 7. M8040A supports data rates up to 32 Gb/s NRZ, 64 Gb/s NRZ, 32 Gbaud PAM4 and 64 Gbaud PAM4. The user interface allows selection of NRZ and PAM4 without reconnecting the BERT test setup.

Master PAM4 Receiver Test Challenges with M8040A

Design and test engineers who need to characterize devices that support PAM4 data formats are facing new test challenges in addition to the signal integrity issues known from 25 Gb/s NRZ device testing.

For PAM4 input receiver tolerance test, this means impairments that may occur in the real-world should be tolerated by the receiver under test without exceeding the desired BER level. Typcial receiver tests include jitter tolerance, interference tolerance test and level sensitivity margins that are applicable for NRZ and PAM4 devices. In addition PAM4 receivers require additional margin testing for level non-linearity, cross-talk effects from adjacent lanes and vertical eye closure.
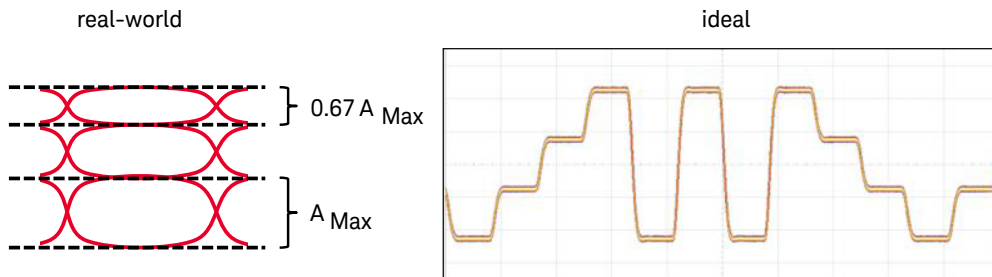
real-world   ideal

Figure 8. PAM4 eyes can show a level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

Real-time Error Analysis for PAM4 and NRZ Signals

Receiver verification checks if the receiver under test operates below the specified BER while emulating the worst-case transmitter and channel conditions.
BER measurements are well established for NRZ signals by using a traditional BERT, but what does this mean for PAM4 signals?

For proper error detection of PAM4 signals, all thresholds (V_{low}, V_{mid}, and V_{upper}) have to be analyzed simultaneously to ensure a correct symbol error measurement. (See Figure 8.) If a "1" is detected at the V_{mid} threshold, the received pattern can have level 2 or 3. Only if the level detected at V_{upp} is checked simultaneously with V_{mid}, it can be determined if the received inputs have the correct level for a 2 or a 3. If two thresholds are errored within one UI, this case translates just into one symbol error.

Detecting	1	0
Threshold V_{upp}	= 3	= 0 or 1 or 2?
Threshold V_{mid}	= 2 or 3?	= 0 or 1?
Threshold V_{low}	= 1 or 2 or 3?	= 0

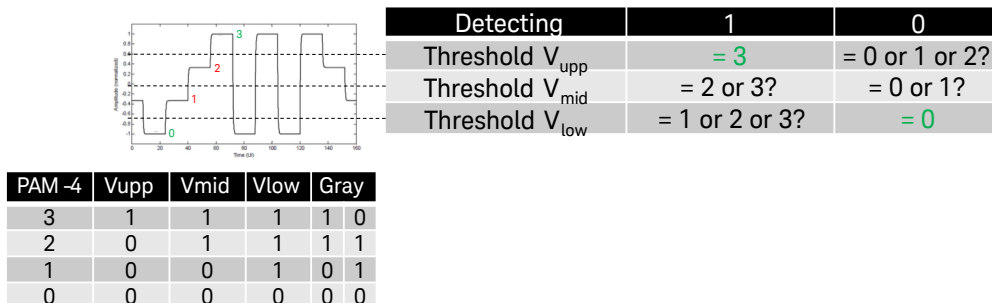| PAM -4	Vupp	Vmid	Vlow	Gray	
3	1	1	1	1	0
2	0	1	1	1	1
1	0	0	1	0	1
0	0	0	0	0	0

Figure 9. Only a true PAM4 error analyzer like M8040A, can provide a PAM4 symbol error rate in real-time without post-processing. Error ratios down to 10^{-15} or error-free can be measured even for long PRBS $2^{31}-1$, QPRBS13-CEI or QPRBS31-CEI patterns. Errored 0,1,2,3 and symbol errors can be counted separately for further debugging.

The M8040A provides real-time error analysis of PAM4 and NRZ signals.
Key capabilities of the error analyzer module M8046A include:

– One differential channel per analyzer module
– Symbol rates from 5 to 30 Gbaud for PAM4 and from 5 to 32 and 64 Gb/s for NRZ
– Native PAM4 decoding
– Built-in equalization to re-open closed eyes at the analyzer input
– Selectable expected patterns like QPRBS31, pattern memory, pattern sequencing, masking, Gray coding and custom PAM4 symbol mapping
– Integrated clock recovery option and control via M8070ADVB of external clock recovery units N1076A/B, N1077A, N1078A
– DUT control interface allows to access built-error counters from the M8070ADVB software package.

Error Distribution Analysis

The Error Distribution Analysis M8070EDAB offers burst error analysis, frame loss ratio estimation and error mapping. Following metrics are calculated for user-definable symbol length, frame length and correctable symbol errors per frame:

– Symbol-error per frame distribution with user-definable symbol and frame length
– Consecutive error distance distribution
– Frame loss ratio, counted and estimated
– Error map provides insight into burst error mechanisms.

The M8070EDAB is a licensed software package that requires a M8070B version 6.0 and higher.

Figure 10. The error distribution analysis M8070EDAB provides multiple views to debug the error distribution. The figure shows an example of symbol errors per frame based on captured pattern streams, with the measured frame loss ratio, based on user-definable number of bits per symbol, correctable symbols per frame and frame length.

Automated Receiver Calibration and Characterization for IEEE 802.3bs, OIF CEI-56G-VSR, PCI Express 5.0, and TBT 3 Interfaces

To simplify the compliance testing and characterization of receiver test, Keysight provides automated receiver test automation software for various electrical and optical interface standards. Here is an overview of test automation software solutions available supporting the M8040A high-performance BERT.

Standard	Interface	Variants	BERT	Test Automation Software
IEEE 802.3bs	Electrical, chip-to-module	400GAUI 200GAUI	M8040A	M8091BSPA Pre-Compliance Receiver Test Automation for IEEE 802.3bs
IEEE 802.3bs	Optical	400GBASE-LR8/-FR8 and 200GBASE-LR4/-FR4/-DR4	M8040A	N4917BSCA Optical Receiver Stress Test Solution
OIF CEI 4.0	Electrical, host and module	56G-VSR PAM4	M8040A	M809256PA Pre-Compliance Receiver Test Automation for CEI-56G
PCI Express 5.0	Electrical	PCIe 8/16/32 GT/s	M8040A	N5991PB5A Receiver Test Automation for PCI Express according to PCI Express 5.0 base specification and N5991PA3A Automated LinkEQ RX and TX testing
TBT 3	Electrical	Thunderbolt 3	M8040A	N5990A-104 TBT3 Receiver Test Automation Software

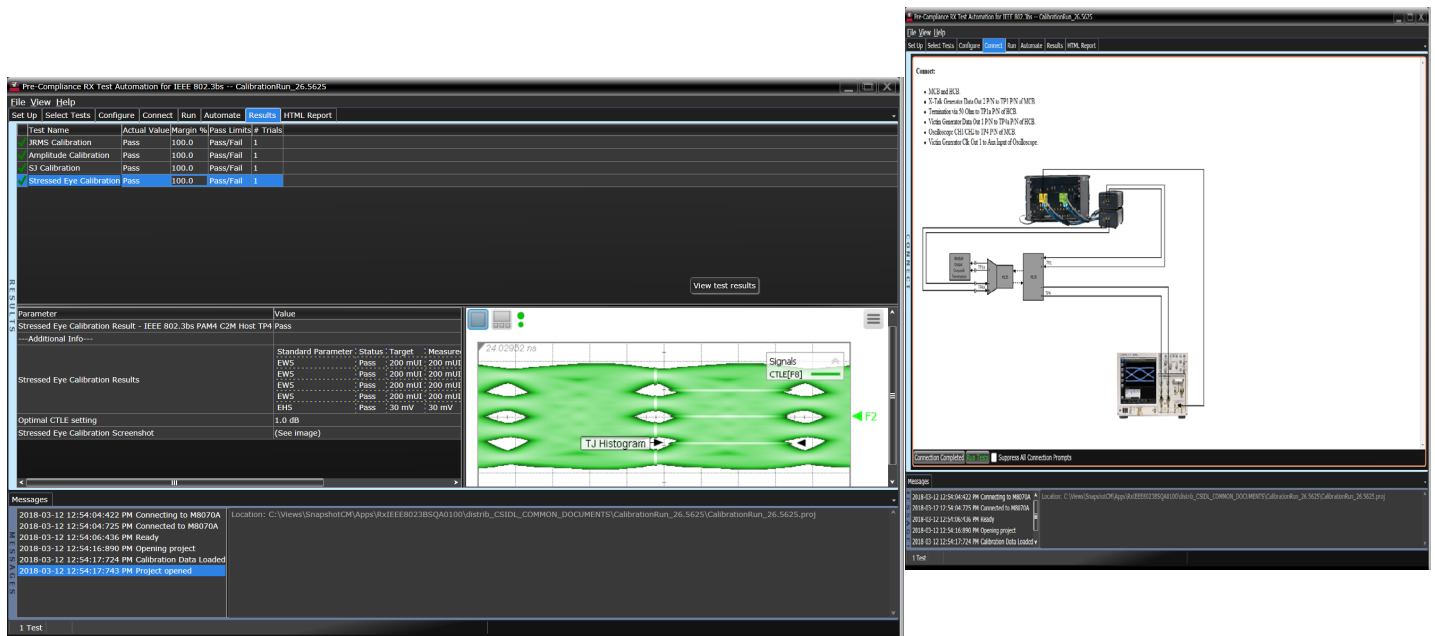Figure 11. Automate the complicated stress signal calibration procedure with guided steps how to connect the test setup and pre-compliance measurements by using the M8091BSPA receiver test automation software for IEEE 802.3bs for chip-to-module interfaces 400GAUI-8 and 200GAUI-4. The figure shows screen shots of the automation software with the results of a successful stress calibration (left side) and guided test setup (right side).

Specifications for M8045A and M8046A Modules and M8057A Remote Head

M8045A pattern generator module for two data channels, 3-slot AXIe

M8045A Pattern generator module for one data channel, 3-slot AXIe

M8057A remote head with cable connections (0.85 m) front and rear view

M8046A analyzer module, 1-slot AXIe

Figure 12. Front panel views of pattern generator module M8045A (top) as 2 and 1 channel (center) versions, remote head M8057A, and error analyzer module M8046A (bottom). To allow a very short connection to the device under test, the remote head is used. One remote head is needed for each of the pattern generator data outputs of M8045A.

Specifications for Pattern Generator Module M8045A and Remote Head M8057A

Data output (DATA OUT 1, DATA OUT 2)

The pattern generator supports symbol rates up to 32 Gbaud or 64 Gbaud, default is one channel and NRZ format.
The remote head M8057A is needed once per channel. Using the P and N outputs of the M8045A without remote head is prohibited.

For the following generator functions a separate module option is required:
- PAM4 coding up to 32 Gbaud (M8045A Option 0P3)
- PAM4 extension to 64 Gbaud (M8045A Option 0P6)
- Second data channel (M8045A Option 0G2)
- Advanced jitter sources (M8045A Option 0G3)
- De-emphasis (M8045A Option 0G4)
- Forward Error Correction (FEC) encoding (M8045A Option 0G9)

Table 1. Data output characteristics for M8045A with remote head M8057A.

All timing parameters are measured @ 0.5 V into ground at data outputs of remote head M8057A	
Symbol rate	2.025 to 32.4 Gbaud for M8045A Option -G32 2.025 to 58.0 Gbaud (all specifications are valid up to 58 Gbaud with over-programming up to 64.8 Gbaud) for M8045A Option -G64
Data format	NRZ (default) PAM4 (requires M8045A Option -0P3 and for symbol rates above 32 Gbaud -0P6 in addition)
Channels per module	1 or 2 (requires M8045A Option -0G2 and second remote head)
Amplitude	
For symbol rates < 32.4 Gbaud	50 mV to 0.9 Vpp single ended 100 mV to 1.8 Vpp differential
For symbol rates < 58 Gbaud	50 mV to 0.6 Vpp single ended 100 mV to 1.2 Vpp differential
Amplitude accuracy	±10% ±10 mV typical (AC) [1]
Output voltage window	−1 to +3.0 V depends on external termination voltage [5]
External termination voltage	−1 to +3.0 V
Transition time [2]	9 ps typical (20 to 80%) for symbol rates > 32.4 Gbaud 11 ps typical (20%-80%) for symbol rates ≤ 32.4 Gbaud
Intrinsic total jitter	8 ps typical @ 32.0 Gb/s NRZ, PRBS 15, BER 10^{-12}
Intrinsic random jitter (NRZ)	5 mUI rms typical @ symbol rates between 2.025 Gbaud and < 22 Gbaud 7 mUI rms typical @ symbol rates between 22 Gbaud and < 32.4 Gbaud 10 mUI rms typical @ symbol rates between 32.4 Gbaud and < 40 Gbaud 12 mUI rms typical @ symbol rates between 40 Gbaud and < 52 Gbaud 10 mUI rms typical @symbol rates between 52 Gbaud and < 58 Gbaud
Data delay range	0 to 10 ns, resolution 100 fs
Data delay accuracy	± (max. (1.5 ps or 10 mUI whatever is higher) + 1% of entered value) typical [3]
Electrical idle	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI.
Skew between normal and complement output	3 ps maximum at the end of the recommended cable pair. Fixed.
Skew between data output ch 1 and data output ch 2	370 ps maximum[4] Repeatability after manual deskew ± 300 ps typical

1. At 5 Gbaud measured with DCA-X N1045A and clock pattern and in the middle of the eye.
2. Measured with DCA-X N1045A.
3. At constant temperature.
4. Requires M8070A software revision 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400
5. High level voltage range= 2/3* V_{term} - 0.95 V < HIL < V_{term} + 2 V
   Low level voltage range= 2/3 * V_{term} - 1 V < LOL < V_{term} + 1.95 V

Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected.
	DC output coupling mode:
	Termination range for devices connected to data out:
	  – Unbalanced 50 Ω +15 Ω / –10 Ω
	  – Typical balanced 100 Ω ±30 Ω typical
	Operation into open is possible for these ranges when DC coupled and balanced termination modes are selected:
	  – Output amplitude max. 300 mV
	  – Offset 0 to 370 mV
	When using AC coupled mode, an internal DC blocking capacitor is applied.

Termination modes	Balanced/unbalanced
Coupling	DC/AC selectable coupling of device under test
Connectors	1.85 mm, female

De-emphasis (DATA OUT)

The M8045A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter see Figure 11. Users can enter the de-emphasis in coefficient values.

Table 2. Specifications for multi-tap de-emphasis (requires Option 0G4).

	NRZ	PAM4
De-emphasis taps	4, can be adjusted for each channel independently	
Pre-cursor coefficient c0	0.0 to ± 0.40 [1]	0.0 to ± 0.40 [1]
Pre-cursor coefficient c1	0.0 to ± 0.40 [1]	0.0 to ± 0.40 [1]
Main cursor coefficient c2	0.0 to ± 1.0 [1]	0.0 to 1.0 [1]
Post-cursor coefficient c3	0.0 to ± 0.40 [1]	0.0 to ± 0.40 [1]
Post-cursor coefficient c4 [2]	0.0 to ± 0.40 [1]	0.0 to ± 0.40 [1]
Cursor coefficient resolution	0.01	0.01

1. Sum of all cursors absolute values may not exceed 1.0 $|c0| + |c1| + |c2| + |c3| + |c4| \leq 1$. Also $|c0|, |c1|, |c3|, |c4| < |c2|$.
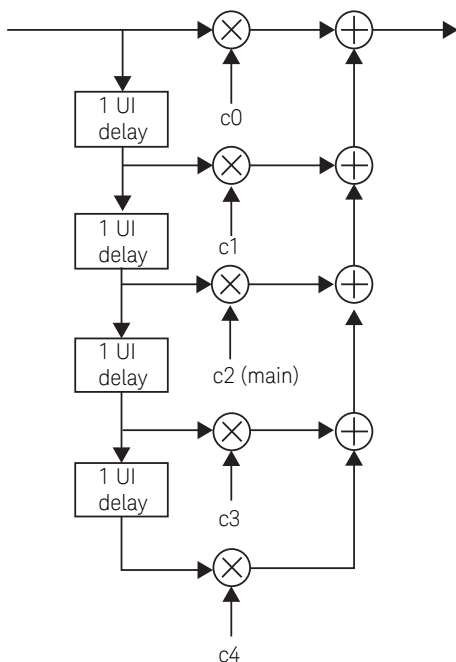2. Requires M8070A software 5.0/M8070B SW 6.0 or later.

Figure 13. The pattern generator of M8045A provides integrated de-emphasis to emulate TX equalization. Two post-cursors c3 and c4, main cursor c2 and two pre cursors c0 and c1 can be adjusted.

Forward Error Correction (FEC) Encoding (Data OUT)

The M8045A pattern generator module supports forward error correction (FEC) and precoding encoding according to IEEE802.3cd. Users can inject pre- and post-FEC errors to test the DUT's devices FEC decoder function.

Table 3. Specifications for FEC (Forward Error Correction) encoding (requires M8045A option 0G9)

FEC encoding	IEEE 802.3cd (draft 3.1) 50GBASE-R
Reed-Solomon Code	RS (544,514)
Scrambler	PRBS 2^{58}-1
Pattern sequence	These patterns from pattern library can be FEC encoded: Remote faults, Scrambled idle
Line coding	PAM4
Number of lanes	1
Symbol rate	26.5625 Gbd PAM4
FEC error injection	Pre-FEC: insertion of a single BIP Post-FEC: FEC symbol errors, randomly distributed, selectable amount of symbol errors per FEC frame
Pre-coder	PAM4: 1(1+D) mod4, can be switched on/off
Pre-requisites	M8045A with option 0P3 and 0G9, M8070A SW 5.1/ M8070B 6.0 or later.

Clock output 1 and 2 (Channel 1 CLK OUT, Channel 2 CLK OUT)

These clock outputs provide two modes. They can operate with the same jitter as the corresponding data output or operate in a clean mode.

Table 4. Specifications for channel 1 clock output and channel 2 clock output.

Frequency range		1.0125 to 16.2 GHz with M8045A-G32 1.0125 to 32.4 GHz with M8045A-G64
Frequency divider factors		Symbol rate / clock divider: 2, 4, 8, 16. Divided output frequency must fit into frequency range
Clean clock mode	On	No jitter injection, no SSC
	Off	Same jitter and SSC as data output of same channel
Amplitude		1 V typical nominal single ended
Duty cycle		50%, accuracy ± 15% typical
Intrinsic random jitter		6 mUI rms typical for symbol rates between 2.025 Gbaud and ≤ 27 Gbaud 10 mUI rms typical for symbol rates > 27 Gbaud. Refers to mUI of symbol rate.
Termination		50 Ω into GND or external termination voltage. Do not operate into open.
Coupling		AC coupled
Connectors		3.5 mm, female

Clock output (CLK OUT)

This is a differential clock output with many sub-rate clock dividers. LF SJ and HF jitter can be turned off and on individually. HF jitter has the same setting as HF jitter of data output of channel 1. Delay on the trigger output also impacts clock output.

Table 5. Clock output specifications.

CLK frequency range		1.0125 to 16.20 GHz
Clock divider in relation to clock frequency range		n * (1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80) with n= 1 < 16.2 GHz n= 2 for 16.2 GHz to 32.4 GHz n= 4 > 32.4 GHz For other dividers use TRIG OUT
Frequency resolution		1 Hz
Frequency accuracy		± 15 ppm
Amplitude	Differential	0.2 to 2.0 V, 10 mV steps
	Single ended	0.1 to 1 V, 5 mV steps
Output voltage window		–1 to +3 V [1]
External termination voltage		–1 to +3 V
Transition times		20 ps typical (20 to 80%)
Duty cycle		50%, accuracy ± 15%
Clock modes		See Table 5
Intrinsic random jitter		300 fs rms typical at 16.2 GHz and clock divider = 1
Jitter injection		LF Jitter: – Can be set independently from Data Out – Has the same LF jitter parameters and ranges as Data Out HF Jitter: – On -> the jitter values from Data Out1 HF Jitter are applied to Clock Out – Off -> no HF Jitter SSC: – SSC is a system-wide parameter and therefore applies to CLK OUT too
SSB phase noise [2]		– 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100 MHz as external reference clock – 80 dBc/Hz typical with 10 kHz offset for reference clock multiplier bandwidth 0.1 MHz
Termination		50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage
Coupling		DC coupled, differential
Connectors		3.5 mm, female

1. If V_{term} is other than 0 V the following applies:
    High level voltage range= 2/3 * V_{term} – 0.95 V < HIL < V_{term} + 2 V
    Low level voltage range= 2/3 * V_{term} – 1 V < LOL < V_{term} + 1.95 V
2. For reference clock multipliers < 400.

Table 6. Clock modes.

Clock mode	Clock generation	Input frequency range
Internal	PLL with internal reference	N/A
Reference	PLL with bandwidth below 1 kHz	10/100 MHz
Direct	No PLL. Maximum symbol rate is 16.2 Gbaud	8.1 to 16.2 GHz
Reference clock multiplier bandwidth 100 kHz	m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620	10 MHz to 16.2 GHz

Supplementary Inputs and Outputs of M8045A

Reference clock input (REF CLK IN)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows using an external clock, see clock modes as shown in table 6. A SSC tolerant PLL is used to multiply the external reference clock to the system clock.

Table 7. Reference clock input specifications (M8045A only).

Input amplitude	0.2 to 1.4 Vpp
Input frequency	10 MHz to 16.2 GHz, depends on clock mode and max. data rate option
Interface	Single ended. 50 Ω nominal
Connector	SMA, female

Trigger output (TRG OUT)

This output is used to send a trigger signal to another connected device, such as an oscilloscope. Also it can be used to generate a subrate clock.

The trigger output can be used in different modes:
1. Divided clock, dividers:
   a. For < 16.2 Gbaud trigger data rate range 2 to 65532
   b. For 16.2 to 32.4 Gbaud trigger data rate range 4 to 65532 with step resolution of 2
   c. For > 32.4 Gbaud trigger output data rate range 8 to 65532 with step resolution of 4
2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

Table 8. Trigger output specifications.

Amplitude	single-ended	0.1 to 1.0 Vpp
	differential	0.2 to 2.0 Vpp
Jitter injection		The injected jitter is always the same as the jitter at the CLOCK OUT
Delay range		0 to 100 ns, resolution 100 fs
Delay accuracy		± (max. (1.5 ps or 10 mUI whatever is higher) + 1 % of entered value) typical [3]
Skew between trigger output and data output ch 1 or ch 2 [2,3,4]		370 ps maximum Repeatability after manual deskew ± 250 ps typical
Output voltage window		−1 to 3 V [1]
External termination voltage		−1 to 3 V
Interface		Differential, 50 Ω
Connector		3.5 mm, female

1. If V_{term} is other than 0 V the following applies:
   High level voltage range= $2/3 * V_{term} − 0.95$ V < HIL < $V_{term} + 2$ V
   Low level voltage range= $2/3 * V_{term} − 1$ V < LOL < $V_{term} + 1.95$ V
2. Requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400
3. At constant temperature
4. Sequencer controlled trigger (use a cable with 3.75 ns delay (~ 865 mm) connected to trigger output)

Reference clock output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ω.
Connector: SMA, female.

Supplementary Inputs and Outputs of M8045A (continued)

Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error addition.

Table 9. Control input specifications.

Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Threshold voltage	–1 V to +3 V
Delay to data output	< 1 ms, Repeatability ±512 UI (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

Control output A and B (CTRL OUT A, CTRL OUT B)

Generates a pulse or static high/low if used from sequencer.

Table 10. Control output specifications.

Amplitude [1]	0.1 to 2 V
Output voltage [1]	–0.5 to 1.75 V
Delay to data output	±512 UI ± jitter amplitude/2 (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles into open.

Communication Link A and B (LINK 1234)

This communication link enables interactive link training with low latency between a M8045A pattern generator channel and a M8046A analyzer module. Requires to use cable M8051A-801 and M8045A with a serial number of DExxx01000 or higher. Older serial numbers can be upgraded (M8045A-UR4, Return-to-Keysight).

Synchronization out (SYNC OUT)

The sync output is a clock output to synchronize additional modules to a common clock. Can be used to sync the M8046A with the system internal clock.

System input A/B (SYS IN A/B)

These are control inputs to synchronize events for the pattern sequencer.

Table 11. System input specifications.

Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Threshold voltage	–1 V to +3 V
Delay to data output	< 1 ms, Repeatability ±512 UI (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	SMA, female

Supplementary Inputs and Outputs of M8045A (continued)

System output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer. A and B outputs are independently controllable.

Table 12. System output specifications.

Amplitude [1]	0.1 to 2 V
Output voltage [1]	−0.5 to 1.75 V
Delay to data output	±512 UI ± jitter amplitude /2 (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	SMA, female

1. When terminated with 50 Ω into GND. Doubles into open.

Auxiliary input (AUX IN)

Not used.

Clock input (CLK IN)

For future use. See reference clock input for direct clock mode.

Jitter Specifications

The M8045A has integrated and calibrated jitter sources. To use the jitter injection the M8045A Option −0G3 is required.

Table 13. Specifications for low frequency periodic jitter (requires Option -0G3 advanced jitter sources).

Low frequency periodic jitter (LF PJ)	Amplitude range	0 to 123.5 UI * symbol rate (in Gbaud) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 40 MHz the maximum
(generated by IQ modulator)		$LF\ PJ = \dfrac{7.792\ UI * 10^{-3} * symbol\ rate}{modulation\ frequency^{1.2}}$
	Frequency	100 Hz to 40 MHz, sinusoidal modulation
	Jitter amplitude accuracy	±2% ± 1 ps typical
	Adjustable	For each data channel independently, same LFPJ for clock and trigger

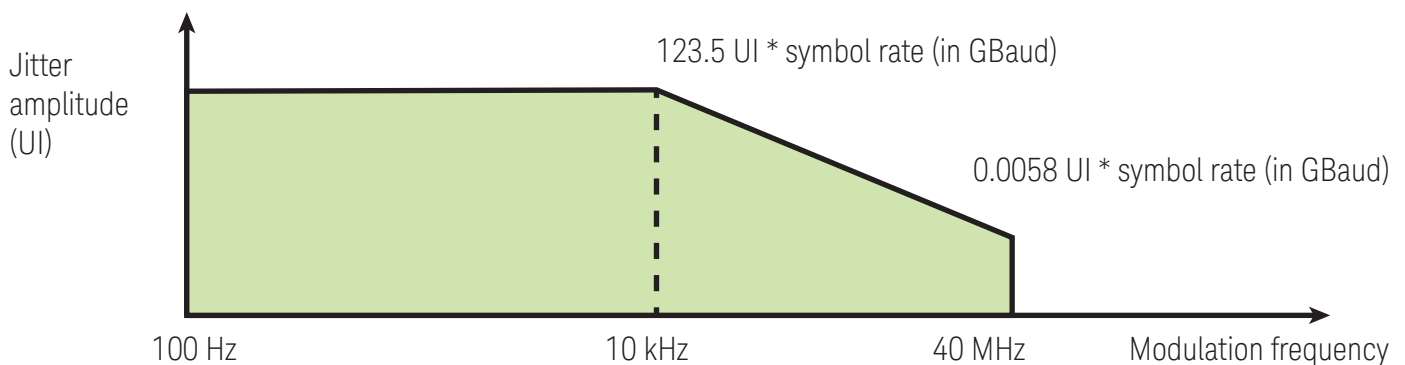## Low frequency periodic jitter

Figure 14. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

Table 14. Low frequency periodic jitter ranges.

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.025 to 4.05 Gbaud	250 to 500 UI	0.0625 to 0.125 UI	0.012 to 0.024 UI
4.05 to 8.1 Gbaud	500 to 1000 UI	0.125 to 0.25 UI	0.024 to 0.048 UI
8.1 to 16.2 Gbaud	1000 to 2000 UI	0.25 to 0.5 UI	0.048 to 0.095 UI
16.2 to 32.4 Gbaud	2000 to 4000 UI	0.5 to 1 UI	0.095 to 0.19 UI
32.4 to 64.8 Gbaud	4000 to 8000 UI	1 to 2 UI	0.19 to 0.38 UI

Table 15. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter, clock /2 jitter (all require M8045A Option -0G3 advanced jitter sources).

High frequency jitter (generated by delay line)	Range	1 UI for > 32.4 Gbaud, for ≤ 32.4 Gbaud minimum of: - 1 UI - 1 UI - (PJ frequency - 250 MHz) / 100 MHz * 0.2 UI - 0.5 UI if RJ low pass filter is 1000 MHz - 0.5 UI if external delay modulation is on Note: This is max sum of RJ, HF-PJ1 and HF-PJ, external delay modulation and BUJ.
High frequency periodic jitter (HF PJ1 and HF PJ2)	Range	See HF jitter above [1]
	Frequency	1 kHz to 500 MHz. For symbol rates < 4 Gbaud the max modulation frequency is symbol rate / 8. Two tone possible. Sweep.
	Jitter amplitude accuracy	±3 ps ± 10% typical [2]
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms (1 UI p-p max.) [1]
	Jitter amplitude accuracy	±300 fs ± 10% typical
	Filters	High-pass: 10 MHz and "off", Low-pass: 100 MHz, Low pass: 500 MHz (for symbol rates ≥ 3.75 Gbaud), Low pass: 1 GHz (for symbol rates ≥ 7.5 Gbaud)
	Adjustable	For each channel independently
	Crest factor	14 (peak-peak to rms ratio)
Spectrally distributed RJ according to PCIe 2 (sRJ) [3]	Range	0 to 72 mUI (1 UI$_{p-p}$) [1]
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	± 300 fs ± 10% typical
	Adjustable	for each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above [1]
	PRBS polynomials	2^n-1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/100/200 MHz low pass 3rd order
	Jitter amplitude accuracy	± 5 ps ± 10% typical for settings shown in Table 15
	Adjustable	For each channel independently
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
Clock/2 jitter	Range	± 50 mUI or ±5 ps typical (whatever is less). Note: this means that first eye can be up to 50 mUI or 5 ps longer or shorter than subsequent eye
	Adjustable	For each channel independently

1. Range of HF jitter applies to sum of RJ, HF–PJ1 and HF–PJ2, external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C
3. Requires M8070B software rev 6.0 or later. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

Table 16. BUJ accuracy applies for these BUJ settings.

BUJ calibration settings [1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2^9–1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2^{31}–1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 17. Specifications for spread spectrum clocking (SSC). Requires M8045A Option -0G3 advanced jitter sources.

SSC (spread spectrum clock)	Symbol rate range for SSC	2.025 to 32.4 Gbaud
	Range	0 to 10,000 ppm (0 to 1%) peak-peak. Select center-spread, up-spread, and down-spread, asymmetric SSC.
	Asymmetric SSC [1]: Upper deviation range Lower deviation range	0 to 1% -1% to 0
	Frequency	100 Hz to 200 kHz
	Modulation	Triangular and arbitrary modulation
	SSC amplitude accuracy	± 0.025% typical
	Outputs	Can be turned on/off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, CLK OUT channel 1/2
Residual SSC [1]	Range	0 to 600 ps
	Frequency	10 to 100 kHz
	Outputs	Can be turned on/off together for CLK OUT, DATA OUT1, DATA OUT2, TRG OUT, CLK OUT Channel 1/2

1. Requires M8070A SW. 5.0/M8070B SW 6.0 or later.

External jitter modulation

An external modulation source can be used to modulate the delay of the M8045A data outputs, clock output and trigger output.

DATA MOD IN 1, 2

This input can be used for delay modulation by an external source for each data output channel individually.

Table 18. Specifications for external jitter modulation on data outputs.

External jitter - data modulation input 1 and 2	Range	Up to 1 UI for symbol rates > 32.4 GBaud Up to 0.5 UI for symbol rates ≤ 32.4 GBaud [1] 0.8 Vpp max
	Frequency	Up to 500 MHz
Gain		1UI/0.725 V ± 5% typical [2]
Linearity		50 mUI
Connectors		3.5 mm, female

1. See HF jitter specifications for the maximum sum of RJ, HF–PJ1 and HF–PJ2 external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

CLK MOD IN

This input can be used for delay modulation of TRIG OUT and CLK OUT, the modulation always affects both outputs.

Table 19. Specifications for external jitter modulation for clock and trigger.

External jitter - clock modulation input	Description	Input for the delay modulation for the TRG OUT and CLK OUT. Affects both
	Range	Up to 1 UI for symbol rates > 32.4 Gbaud Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud [1] 0.8 Vpp max
	Frequency	Up to 500 MHz
Gain		1 UI/0.725 V ± 5% typical [2]
Linearity		50 mUI
Connectors		SMA, female

1. See HF jitter specification for the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C

External level interference (RI/SI) sources

The Keysight M8054A interference source, and M8195A and M8196A AWG can be used as level interference source with sinusoidal and random modulation. The M8000 system software controls the interference parameters such as amplitude, bandwidth, crest factor. Keysight provides a matched directional coupler pair for injecting the RI or SI signal before or after the channel. See table below.

Table 20. Specifications for external level interference sources RI/SI with M8195A, M8196A, and M8054A

	M8070A parameters	M8195A	M8196A/M8054A [2]
Random Interference (RI)		Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	80 mV to 1 V	80 mV to 1 V
	Lowest frequency range	320 kHz -20 GHz (ch1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
	Highest frequency range	320 kHz to 25 GHz	160 kHz to 32 GHz
	Crest factor (peak ratio)	> 4	> 4
Sinusoidal interference (SI)		Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	80 mV to 1 V	80 mV to 1 V
	Frequency range	320 kHz -25 GHz (channel 1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
Common mode sinusoidal interference (CMSI) [1]		Yes	Yes
	Amplitude	0 to 995 mV	0 to 995 mV
	Modulation frequency range	1 MHz to 12 GHz	1 MHz to 12 GHz
	Phase range	-360 to 360 deg	-360 to 360 deg
Differential mode sinusoidal interference (DMSI)		Yes	Yes
	Amplitude	0 to 995 mV	0 to 995 mV
	Modulation frequency range	1 MHz to 12 GHz	1 MHz to 12 GHz
	Phase range	-360 to 360 deg	-360 to 360 deg
Simultaneous injection of CMSI and DMSI [1]	Simultaneous injection of CMSI and DMSI [1]	0 to 995 mV	0 to 995 mV
Recommended accessories	M8045A-802 Matched directional coupler pair, 50 GHz, 13 dB, 2.4 mm (recommended for RI and higher BW), M8045A-803 Matched coupler pair, 40 GHz, 12 dB, 2.4 mm (recommended for PCIe5, CMSI, DMSI)		
Software pre-requisites	M8070A SW 4.0/M8070B SW 6.0 or higher	M8195A firmware V3.2.0 or higher	M8196A firmware V2.1.0.0 or higher M8054A firmware: TBD

1. Requires software revision 5.0 or later
2. Call factory for availability.

ISI channels (intersymbol interference) with M8049A

External ISI channels are available to emulate channel loss. Keysight M8049A provides 3 different ISI boards with various insertion loss characteristics. M8049A-001 provides 5 short traces, M8049A-002 has 9 medium length traces and M8049A-003 offers 7 long traces. For detailed specifications see M8049A data sheet.
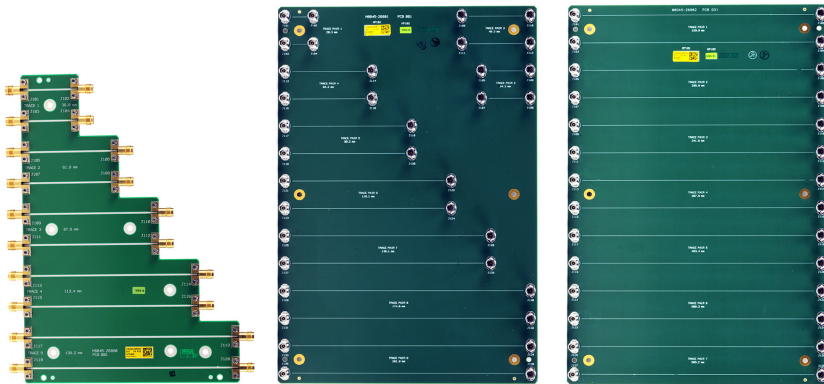

Figure 15. Emulate channel loss for receiver margin testing with Keysight's ISI channel boards.

Pattern Sequencer, Filler Symbol Filtering, and Interactive Link Training

Table 21. Specifications for pattern, sequencer.

PRBS [1]	2^n-1, n= 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51, 58
PRBS	2^n, n = 7, 10, 11, 13, 15, 23
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q, SSPRQ
New patterns in library	PAM4-linearity, JP03A, JP03B
PAM4 coding	Gray coding, custom mapping of 00, 01,10,11 to symbols 0,1,2,3
Mark density	PRBS 1/8 to 7/8
Zero substitution	Yes
Export/Import	Patterns from M8000 and N4900 series can be imported
Pattern library	Yes
User definable memory	NRZ: 2 Gbit/channel, PAM4: 1 Gsymbol/channel
Vector/sequence granularity	512 bit
Pattern capture	Yes, raw data for PAM4 Capture data starts on event – User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols – Events: error, CTRL IN A /B, immediate – Max 2 Gbit/ch capture data for NRZ, 1 Gsymbol/ch for PAM4 Save captured data: – With errors – As expected data (ignores error content) – As PG data (ignores error content) – Export via pattern editor windows – Convert bits into all other codings and vice versa – Ability to mask error bits automatically Display of captured data: – Display errors with color coding Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. Polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx series.
2. M8045A only

Filtering of SKP OS (M8046A Option -0S2)

SKP OS filtering is required whenever a device under test (DUT) modifies the SKP Ordered Sets embedded in the test pattern. This is always the case when the DUT is operated in independent reference clock (IR) mode but dependent on the DUT's loop back implementation it can happen in common reference clock (CC) mode as well. Whenever SKP OS filtering is enabled it is required to use a test pattern version including SKP OS in the pattern generator sequence and an expected test pattern version without SKP OS in the error detector sequence. Respective patterns are part of the factory pattern library. This functionality requires M8046A-0S2 and a M8070B software revision 6.0 or later.
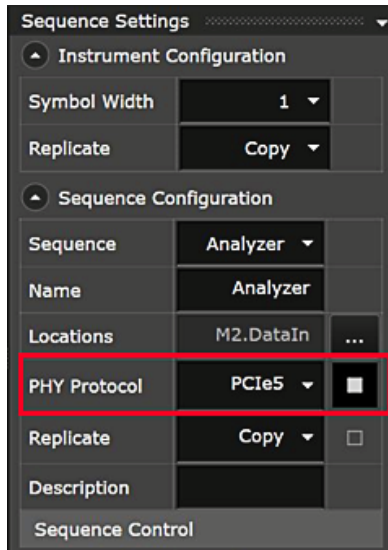
Figure 16. Select PCIe5, PCIe4, PCIe3 or CCIX as PHY protocol to enable the SKP OS filtering with M8046A-0S2.

Interactive link training for PCIe

In some industry standards, such as PCIe, the transmitter de-emphasis and receive equalization have to be optimized during a training sequence to compensate for the actual channel loss caused by PC board materials.

For testing receivers of such interfaces, you need an error analyzer that understands the low-level protocol of the bring-up sequence including speed changes and triggering changes of the pattern generator's de-emphasis setting.

M8046A provides a link training status state machine that supports PCIe 8, 16, and 32 GT/s. It is suitable to test the root complex and end point. Supports 2 channels.
Pre-requisites for this functionality:

– Module hardware: M8046A Option -0S1. Requires M8045A and M8046A modules with a high-speed communication path (LINK 1234), which are available for all serial numbers of DExxx01000 or later. M8046A-0A4 integrated clock recovery and a pattern generator with M8045A-0G4 de-emphasis is also required. M8046A-0S2 is recommended.
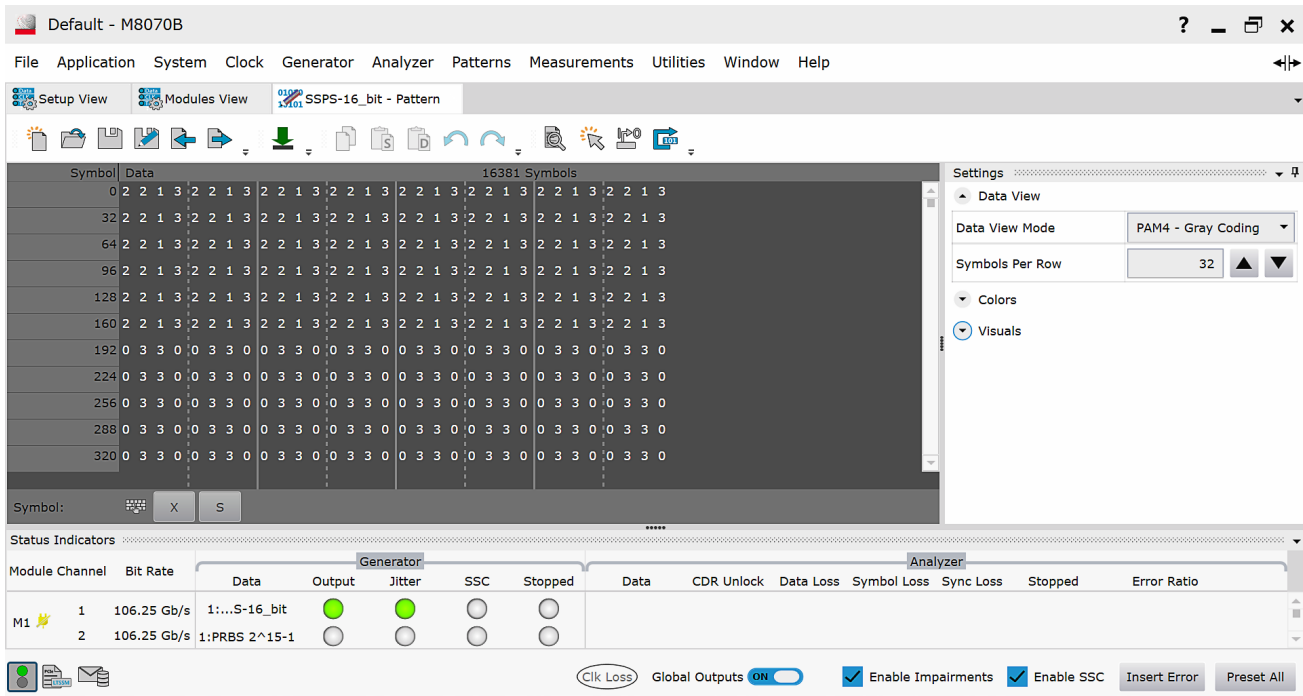– Software: M8070B rev 6.x. Contact factory for availability.

Figure 17. The pattern editor in the M8070B software allows editing NRZ bits and PAM4 symbols. The PAM4 symbol to bit mapping can be selected as Gray coded or custom with adjustable PAM4 levels. Quaternary PRBS, like QPRBS13-CEI or QPRBS31, according to CEI and IEEE standards can be selected as well as SSPRQ and PAM4 linearity test patterns.

Specifications Analyzer Module (Error Detector) M8046A

Figure 18. Front panel of M8046A

The M8046A supports symbol rates up to 32 Gbaud and 64 Gbaud, the default is 32 Gbaud and NRZ format.
The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator and the M8195A/M8196A arbitrary waveform generator. For the following functions a separate module option is required:
  – PAM4 decoding up to 32 Gbaud (M8046A Option -0P3)
  – Equalization for symbol rates above 32.4 Gbaud (M8046A Option -0A3)
  – Analyzer, 1 channel, data rate up to 64 Gbaud, NRZ (M8046A Option -A64)
  – Clock recovery up to 32 Gbaud (M8046A Option -0A4), extension to 64 Gbaud (M8046A Option -0A5)
  – Interactive link training for PCIe 8/16/32 GT/s (M8046A Option -0S1)
  – SKP OS Filtering for PCIe 8/16/32 GT/s and CCIX 20/25 Gb/s (M8046A Option -0S2)

Data input (DATA IN)

Table 22. Specifications for analyzer/error detector.

Symbol rate	5.0 to 32.4 Gbaud NRZ for M8046A-A32 5.0 to 30 Gbaud PAM4 for M8046A-A32 with -0P3 5.0 to 64.8 Gbaud NRZ for M8046A-A64
Channels per module	1
Data format	NRZ (default) PAM4 (requires M8046A Option -0P3)
Max # of M8046A per M9505A chassis	up to 4
Input sensitivity [1, 3]	12% of input range setting + 40 mV per eye, single ended and differential. For modules with a serial number below DExxx00515 these specifications apply: NRZ: 70 mV single ended and differential PAM4: 70 mV per eye single ended and differential
Max input voltage amplitude	1600 mVpp differential for balanced patterns. For modules with serial number below DExxx00515: 1000 mVpp differential
Input voltage window	-1 V to +3 V
Termination voltage [5]	-1 V to +3 V for modules with serial number above DExxx00515
Timing resolution	0.1 ps
Input bandwidth	16 GHz typical
Sampling point	Manual and automatic. Finds optimum voltage range, threshold and delay of the sampling point. Delay accuracy is 20 mUI or 1.5 ps whichever is higher. [4] One sampling edge per UI.
Decision threshold range	Full input voltage range with 1 mV resolution
Input equalizer	For symbol rates up to 32 Gbaud: Up to 13 dB at 32.4 Gbaud NRZ Up to 5.5 dB at 29 Gbaud PAM4 Up to 5.1 dB at 26.5625 Gbaud PAM4 FFE with 55 presets for PAM4 and 120 presets for NRZ. See figure below. No Equalizer license is needed below 32 Gbaud. For symbol rates above 32 Gbaud: Up to 3 dB at 58 Gb/s for NRZ signals. (requires M8046A-0A3 and -A64): 120 presets for NRZ, FFE.
Phase margin [2] NRZ	1 UI – 12 ps typical for PRBS 2^{15}– 1 1 UI – 8 ps typical for clock pattern
PAM4	1 UI – 34 ps typical for PRBS 2^{15}– 1
Interface	Differential: 100 Ω, Single ended: 50 Ω DC coupled, terminate unused input with 50 Ω For modules with a serial number below DExxx00515: AC coupled, terminate unused input with 50 Ω
Connectors	2.4 mm, female

1. Measured with PRBS 2^{31} – 1 at 32.4 Gb/s NRZ or 30 Gbaud PAM4, at BER of 10^{-12}.
2. Measured at 26.5625 Gbaud and BER of 10^{-12}.
3. Valid at room temperature.
4. With 48 to 52% duty cycle at CLK IN signal.
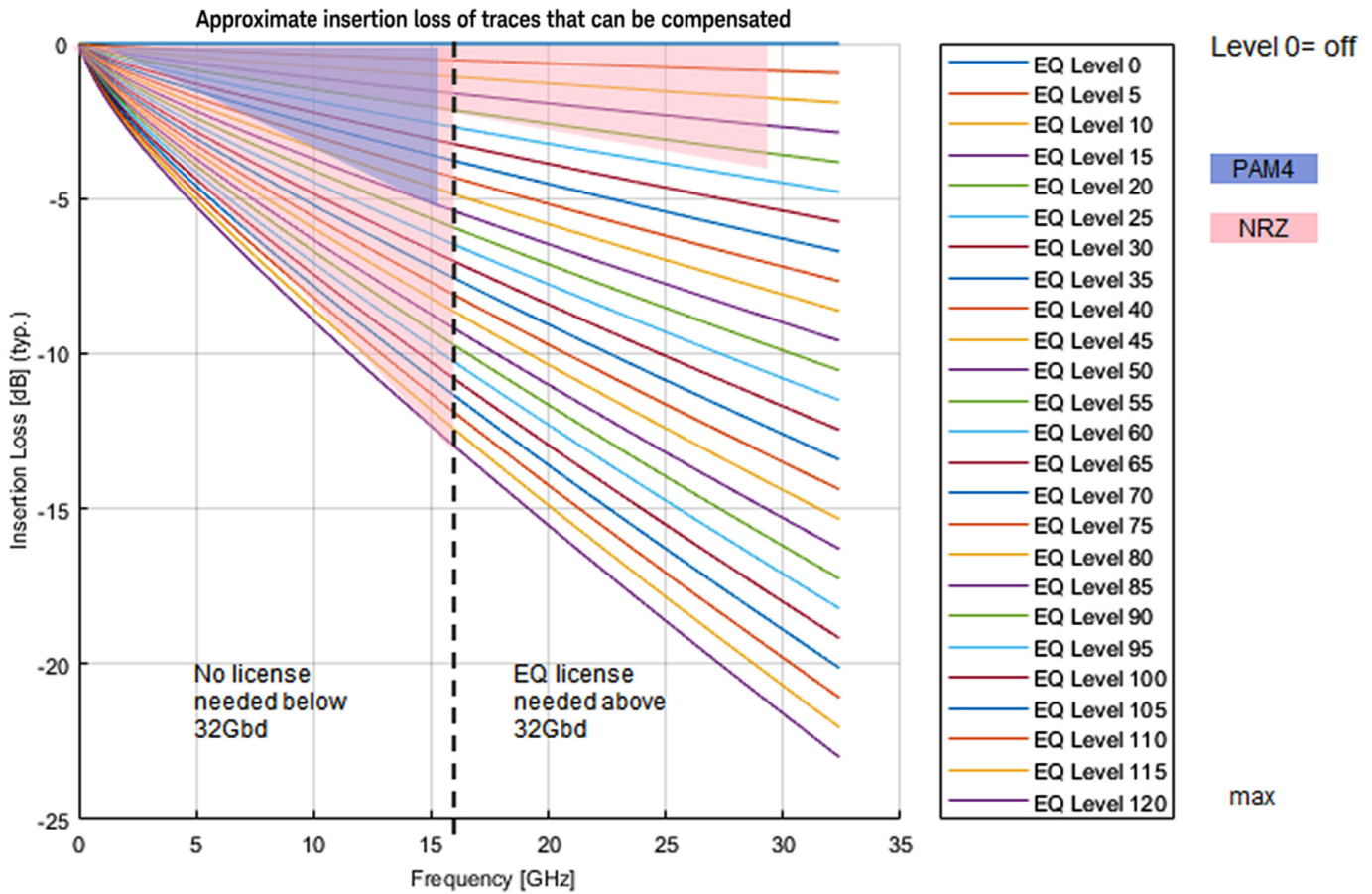5. Termination voltage must be within a window of DC common mode voltage ± 1.5 V.

Figure 19. The M8046A provides built-in equalization to compensate for loss in the loop back channel. The available ranges for PAM4 and NRZ signals up to 64 Gbaud are shown here. For symbol rates above 32Gbd the M8046A-0A3 equalizer option is required.

Table 23. Specification for integrated clock recovery (requires M8046A option UA4, UA5)

	Comment	M8046A Option 0A4/UA4
CR symbol rate range		NRZ: 5 to 32.4 Gb/s (requires M8046A option -0A4) NRZ: 5 to 64.8 Gb/s (requires M8046A options -0A4 and -0A5) PAM4: 5 to 30.0 Gb/s (requires M8046A option -0A4 and -0P3)
Selectable loop type	First and second order PLL - see figure below for description	Yes
Tunable loop bandwidth		2 to 20 MHz
Loop bandwidth accuracy		± 30% typical
Transition density		25-100%
Clock recovery peaking range		Up to 4 selectable settings (dependent on loop bandwidth)
Acquisition range	Input symbol rate must be within the range of ± 500 ppm of the set symbol rate	± 500 ppm typical
Tracking range	SSC can be tracked when symbol rate is set to center frequency. SSC frequency ≥ 30 kHz	± 3000 ppm typical (for symbol rate up to 32 Gbaud)
CDR freeze		Not provided

First order PLL (type 1)

– A type 1 is defined by bandwidth. No peaking.
– JTF bandwidth = OJTF bandwidth.
– Used by some communication standards
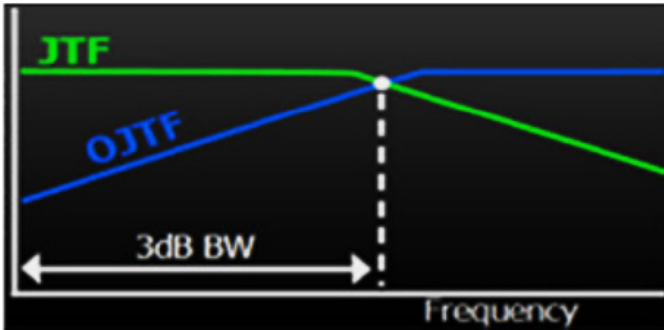
Second order PLL (type 2)

– A type 2 is defined by JTF loop bandwidth and peaking.
– JTF bandwidth > OJTF bandwidth.
– Used by some computing standards
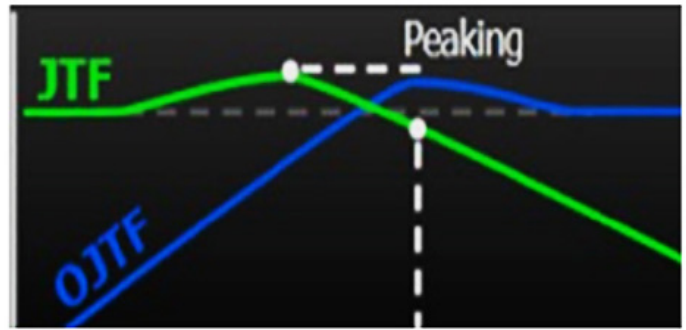
Figure 20. The M8046A provides a built-in clock recovery option. You can choose between a first and second order PLL characteristic.

External clock input (CLK IN)

Table 24. Specifications for clock input of analyzer.

Amplitude	Minimum 200 mVpp, maximum 1 Vpp
Frequency range [1]	2.5 to 32.4 GHz Note: In clk "x 2" mode for symbol rates above 25 Gbaud an external bandpass filter (M8061A-803) has to be used on the clock input. The filter has to be removed for symbol rates below 25 Gbaud. In clk "x 1" mode no filter is needed.
Multiplier internal	1, 2
Connector	3.5 mm, female

1. below 5 GHz transition time of clock signal should be < 25 ps.

Recovered clock output (REC CLK OUT)

This output provides a recovered clock when using the integrated clock recovery function of M8046A. It can be used to trigger a DCA sampling oscilloscope. It is only provided for M8046A modules with S/N above DExxx1000.

Table 25. Specifications for recovered clock output of analyzer.

Amplitude	Fixed 600 mVpp typical
Symbol rate < 32.4 Gbaud	Symbol rate at data inputs/2 (maximum of 16.2 GHz)
Symbol rate < 32.4 Gbaud	Symbol rate at data inputs/4 (maximum of 16.2 GHz)
Connector	3.5 mm, female

SYNC input (SYNC IN)

Can be used to clock the analyzer from the pattern generator's M8045A system clock via the sync output A/B (requires cable M8051A-801). Not needed if external clock is used. This input is only available for M8046A modules with a serial number below DExxxx01000.

Control input A (CTRL IN A)

Functionality can be selected as: sequence trigger, pattern capture event.

Table 26. Specifications for control inputs of analyzer.

Input voltage	–1 to +3 V
Termination voltage	–1 to +3 V
Threshold voltage	–1 to +3 V
Response time	± 512 UI repeatability
Connector	3.5 mm, female

Control output (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Table 27. Control output specifications for M8046A.

Amplitude	0.1 to 2 V
Output voltage	–0.5 to 1.75 V
Delay from data input	< 1 ms, Repeatability ±512 UI (requires M8070A software 4.5/M8070B 6.0 or later)
Connector	3.5 mm, female

Communication link (LINK 1234)

This communication link provides a low latency communication path between M8045A and M8046A modules for enabling interactive link training, e.g. for 8/ 16/ 32Gb/s PCIe. It requires the cable M8051A-801. This interface is available for M8046A modules with a serial number above DExxx01000. Upgrades are available for older serial numbers and require return to Keysight.

Measurements

Table 28. Measurement capabilities.

		M8070A	M8070B	M8070ADVB	M8070EDAB
BER, SER	Accumulation and instantaneous	Yes	Yes		
Jitter tolerance		Yes	No	Yes	
BERT Scan with RJ, DJ separation		No [2]	No	No [2]	
Output level and Q-factor		No	No	No	
Sampling point view		Yes [1]	Yes		
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bits, errored 1 bits Compared symbolds, errored symbols Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3	Yes	Yes		
BER versus parameter automated sweep		Yes	No	Yes	
Error distribution analysis		No	No	No	Yes

1. Requires M8070A SW 4.0/M8070B SW 6.0 or later.
2. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in case of NRZ and invalid in case of PAM4 signals.

External clock recovery

The Keysight N1076A/B, N1077A, N1078A electrical and optical clock recovery units can be used to recover a clock from NRZ and PAM4 patterns to clock the M8046A error analyzer. The clock recovery units can be controlled from the M8000 system software for BER and jitter tolerance testing.

Table 29. Conditions for use of external clock recovery.

	N1076A/77A	N1076B/78A
Symbol rate	NRZ: 5.0 to 32.4 Gb/s PAM4: 5.0 to 30.0 Gbaud	NRZ: 5.0 to 64 Gb/s PAM4: 5.0 to 30.0 Gbaud
Sensitivity with recommended accessories	30% of input range + 45 mV for M8046A with serial number above DExxx00515 (single ended and differential). For M8046A modules with a serial number below DExxx00515 these specifications apply: NRZ: 200 mV PAM4: 120 mV per eye	
Number of consecutive symbols without transition	NRZ: 144 PAM4: 72 (144 bit)	
Measurements	Jitter tolerance, BER	
Software pre-requisites	M8070A 3.6 or higher N1010A Flex DCA A.05.61 or higher, no extra licenses needed	M8070B 6.0 or later and M8070ADVB N1010A Flex DCA A.05.80 or higher, no extra licenses needed
	Note: The M8070A/B and the N1010A controlling the external clock recovery units should run on the same controller. The N1010A Flex DCA software cannot be operated interactively while being controlled by M8070A/B. If a DCA-M is used in the same test setup, we recommend to controlling it from a second PC/controller.	
Hardware pre-requisites	N1076A-232 or N1077A-232 for symbol rates above 16 Gbaud M8046A-A32 with serial number above DE xxx00200.	For symbol rates above 32 Gbaud: N1076B-264/N1078A-264 and M8046A-A64
Recommended accessories (for differential signals)	– Qty 1 of Keysight N1027A-2P2 microwave pick-off tee, 2.4 mm connectors, matched pair – Qty 2 of Keysight 11900B adapter 2.4mm (f) to 2.4mm (f)	For rates above 32 Gbaud: – Qty 1 of Keysight N1027A-2P1 microwave pick-off tee, 1.0 mm connectors, matched pair – Qty 2 of Keysight 11921B adapter 1mm (m) to 1.85mm (f) – Qty 2 of Keysight 11921F Adapter 1.85mm (f) to 1.0 mm (f) — For rates below 30 Gbaud: – Qty 1 of Keysight N1027A-2P8 microwave pick-off tee, 1.85 mm connectors, matched pair – Qty 2 of Keysight 11900B adapter 2.4mm (f) to 2.4mm (f)
	– Qty 2 of Keysight 83059A adapter 3.5 mm (m) to 3.5mm (m) for mounting the pick-off tee directly to inputs of N107xA/B – Qty 1 of Keysight M8046A-802 matched cable pair 2.4 mm, 2 ps	

Error Analysis of PAM4 Signals Using a UXR–Series or DSAZ634A Oscilloscope

Error analysis of PAM4 signals can be done with an error detector such as M8046A with all its advantages as described above. For analyzing the errors of PAM4 signals with symbol rates above 30 Gbaud, the M8000 system software rev 4.0 or higher supports using a Keysight real-time oscilloscope such as DSAZ634A or UXR series for capturing the signal and decoding it into a pattern stream. The M8000 system software can upload the acquired pattern and handle the synchronization and comparison with an expected pattern even for long PRBS polynomials such as PRBS31Q. This method allows measuring target BERs up to of 10^{-6} for symbol rates up to 58 Gbaud within reasonable measurement times (~ 1minute) and using the adjustable equalization and clock recovery functions of the oscilloscope. See table below for more details.
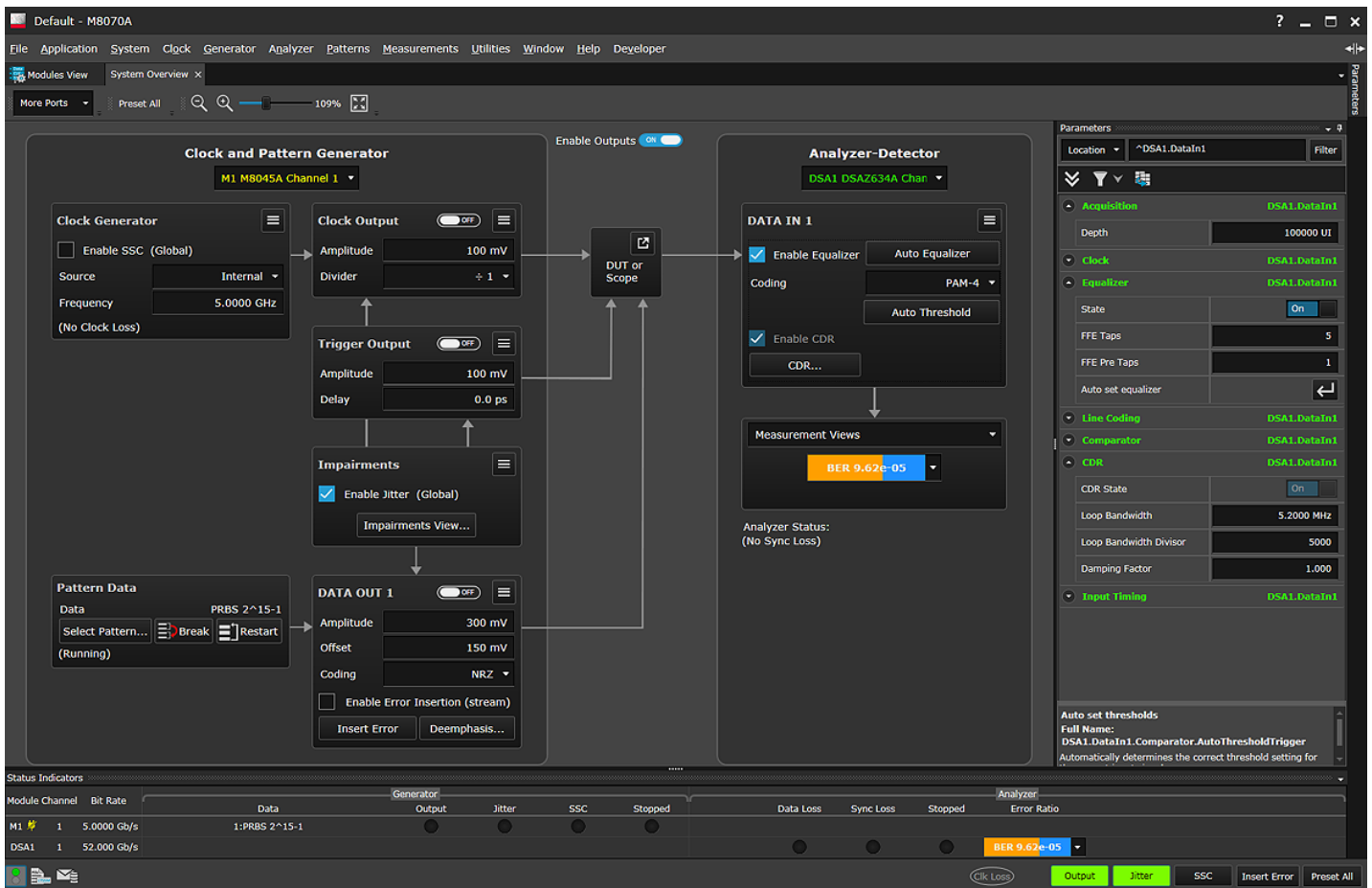
Figure 21. The setup view of the M8070B system software displays all major BERT pattern generator and error analyzer parameters at a glance. The example shows the Analyzer-Detector is using the Keysight DSAZ634A real-time oscilloscope for error analysis of a 52 Gbaud PAM4 signal. At the right you can adjust the acquisition, equalizer, clock recovery parameters of the connected DSAZ634A or UXR.

Table 30. Conditions for error analysis with M8070A/M8070B with M8070ADVB using a real-time oscilloscope.

Symbol rates	14 to 58 Gbaud PAM4 for DSAZ634A with real edge inputs. 14 to 32 Gbaud PAM4 for UXR0334A
Target BER	10^{-6}
Coding	PAM4, NRZ
Expected patterns	User definable: PRBS 2^n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	Jitter tolerance, BER and SER
Measurement time	Depends on: – Expected pattern type – Expected pattern length (in case of memory patterns) – Symbol rate – Equalizer usage and parameters – Acquisition depth in UI – Target BER and confidence level

BER and symbol counters	BER counters
	  – Compared bits
	  – Errored bits
	  – Compared 0 bits, compared 1 bits
	  – Errored 0 bits, errored 1 bits
	Symbol counters:
	  – Compared symbols
	  – Errored symbols
	For each symbol level:
	  – Compared symbols
	  – Errored symbols

Parameters	Acquisition
	Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.)
	  – Global acquisition bandwidth limit
	  – Channel bandwidth limit and filter type
	  – Pattern capture up to 100 Mbit
	Horizontal reference clock: internal, external 10 MHz and 100 MHz
	Clock: Follow Sys Clock, symbol rate
	Line Coding
	  – Coding (NRZ / PAM4)
	  – Symbol mapping (uncoded, Gray, custom)
	  – Custom symbol mapping
	Comparator
	  – Compare mode (single ended / differential)
	  – Polarity (non-inverted / inverted)
	  – Auto-set thresholds
	  – User-defined thresholds
	Equalizer (Feed Forward Equalizer)
	  – Number of taps
	  – Number of pre-taps
	  – Auto-set coefficients
	Clock Recovery (2nd Order CR)
	  – Loop bandwidth
	  – Symbol rate divider
	  – Damping factor
	Sample delay (PAM4 only)
	Auto alignment
	  – Covers thresholds, sample delay and equalizer coefficients
	Automatically set scope parameters
	  – Thresholds
	  – FFE coefficients (cannot be changed by user)
	  – Sample delay position (in case of NRZ)

Supported real-time oscilloscope models	– Keysight UXR0334A – Keysight DSOZ634A, DSAZ634A – Keysight DSOX96204Q, DSAX96204Q – Keysight DSAZ594A *, DSOZ594A * Note: Z-Series oscilloscope needs real-edge inputs. Models with bandwidth < 64 GHz impact the maximum symbol rate * require M8070A SW version 4.5 or higher

Software pre-requisites	**DSO/DSA (Z-series)**	**UXR**
	M8070A SW version 4.5 or higher	M8070B system software for M8000: version 6.0 or higher M8070ADVB
	Minimum supported Infiniium version is 06.10.00616	Minimum supported Infiniium version is 10.00.03902

	Following licenses are required on the oscilloscope in addition:
	  – N5384A Serial Data Analysis (SDA)
	  – N8827A PAM4 Measurement (PM4)
	  – N5461A Equalization (DEQ)
		Following licenses are required on the oscilloscope in addition:
		  – D9010PAMA Pulse Amplitude Modulation PAM-N Analysis Software
		  – D9020ASIA Advanced Signal Integrity Software (EQ, InfiiniSimAdv, Crosstalk)

User Interface and Remote Control

The M8070B system software for the M8000 Series of BER test solutions is required to control the M8040A BERT.

Figure 22. The graphical user interface offers multiple views that can be defined by the user. This example shows the system view on the left side and the pattern generator data output with the PAM4 coding and level linearity parameters at the right.

Table 32. User interface and remote control interface.

System software	M8070B
Controller requirements	Embedded PC: Choose M8040A-BU1 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 7, 8 or 10, 8 or 16 GB RAM, SSD. External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit), Windows 10 (64 bit) Version 1607 (Anniversary Update) or newer (for detailed requirements refer to M8070B release notes)
Controller connectivity with AXIe chassis	USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC)
Programming language	SCPI. Not compatible with N4900 Series and ParBERT 81250A
Remote control interface	Desktop or Laptop PC: LAN M9537A: LAN
Save/Recall	Yes
Display resolution	Minimum requirement 1024 x 768
Software pre-requisites	Microsoft Win 7 SP1 or 8 / 8.1, 10, Keysight IO library rev. 17.2.20605 or above AXIe Chassis Firmware (Embedded System Module (ESM) from Keysight Technologies) version 1.3.42 or above
Software download	See http://www.keysight.com/find/m8070b for latest version

Table 33. Functions provides by the Advanced Measurement software package.

Advanced measurement	M8070ADVB
Measurements	See table measurements
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	External clock recovery units, e.g. N1076A, N1076B, N1077A, N1078A Real-time oscilloscopes, e.g. DASZ634A, UXR0334A
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
SCPI recorder	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: – Parameter changes – Sequence and pattern configuration – Measurement creation, configuration and execution – Group configuration – Save and recall of settings The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT.
Software pre-requisites	M8070B version 6.0 or later
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or time-based with 6/12/24 month duration. The network license is only recommended when using multiple M8040A setups within one company.

Table 34. Functions provides by the Error Distribution Analysis software package M8070EDAB.

Error distribution analysis	M8070EDAB
Measurements	– Frame loss ratio estimation – Error map – Symbol-errors per frame distribution – Consecutive error distance distribution
Software pre-requisites	M8070B version 6.0 or later
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration. The network license is only recommended when using multiple M8040A setups within one company.

# General Characteristics and Physical Dimensions

Modules M8045A and M8046A

Table 35. General characteristics for M8045A and M8046A modules.

	M8045A	M8046A
Operating temperature	5 to 40 °C (41 to + 104 °F)	
Storage temperature	–40 to +70 ºC (modules) (–40 to + 158 °F)	
Operating humidity	15 to 95% relative humidity at 40ºC (non-condensing)	
Storage humidity	24 to 90% relative humidity at 65ºC (non-condensing)	
Power requirements (module only)	Single channel: 515 W Dual channel: 605 W	238 W
Physical dimensions for modules (W x H x D)	3-slot AXIe module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch)	1-slot AXIe module: 351 x 30 x 309 mm (13.8 x 1.8 x 12.2 inch)
Physical dimensions for M8040A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 462 x 193 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8045A module: single channel 6.9 kg (15.2 lb) M8045A dual channel: 7.5 kg (16.5 lb) With M8040A-BU1: 25 kg (55 lb) With M8040A-BU2: 21 kg (46.3 lb)	M8046A module: 3.6 kg (8.0 lb) In bundle with M8045A and in a 5-slot chassis: 24.6 kg (54.3 lb)
Weight shipping	M8045A module: 11 kg (24 lb) With M8040A-BU1: 37 kg (82 lb) With M8040A-BU2: 33 kg (73 lb)	M8046A module: 7.5 kg (16 lb) In bundle with M8045A and in a 5-slot chassis: 37.6 kg (83 lb)
Recommended recalibration period	1 year	
Warm-up time	30 minutes	
Cooling requirements	Slot air flow direction is from right to left. When operating the M8045A /46A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality management	ISO 9001, 14001	

Remote head M8057A

Table 36. General characteristics for M8057A remote head.

	M8057A
Operating temperature	5 to 40 °C (41 to + 104 °F)
Storage temperature	−40 to +70 °C (modules) (−40 to + 158 °F)
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Physical dimensions (W x H x D)	Remote head 117 mm x 68 mm x 185 mm, (4.6" x 2.7" x 7.3")
Physical dimensions for remote head with cable	Length of cable connection between M8057A and M8045A module: 85 cm

M8045A   85 cm   M8057A   15 cm
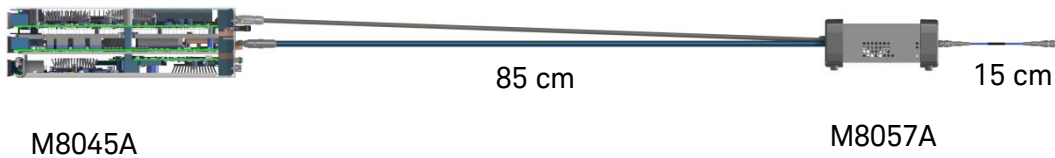
Weight net	1.7 kg (3.75 lb)
Weight shipping	6.5 kg (14.4 lb)
Recommended recalibration period	1 year
Warm-up time	30 minutes
EMC	IEC 61326-1
Quality management	ISO 9001, 14001

Specification Assumptions

The specifications in this document describe the instruments' warranted performance. All specification in this revision of the data sheet are preliminary. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8045A specifications if not otherwise stated are valid at the end of the cable M8045A-801.

All M8046A specifications if not otherwise stated are valid using the recommended cable pair M8046A-802 (2.4 mm matched cable pair). Preliminary specifications are written in italics.

Ordering of M8040A High-performance BERT 64 Gbaud

The M8040A is scalable and upgradeable. The following table shows all available options. Upgrade options are shown below.

Description	Product #	Option	Comment
High-performance BERT 64 Gbaud (systemizing number for factory pre-installation)	M8040A		
Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe	**M8045A**		
Pattern generator one channel NRZ, data rate up to 32 Gbaud (requires remote head, M8057A)	M8045A	G32	One of these is required
Pattern generator one channel NRZ, data rate up to 64 Gbaud (requires remote head, M8057A)	M8045A	G64	
Second channel, hardware and license (requires remote head, M8057A)	M8045A	0G2	
Advanced jitter sources for receiver characterization, module-wide license	M8045A	0G3	
De-emphasis, module-wide license	M8045A	0G4	
Forward Error Correction (FEC) encoding, module-wide license	M8045A	0G9	
PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	0P3	
Extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	0P6	Only with G64 and 0P3/UP3
Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps	M8045A	801	Qty 2 recommeded
Remote head for M8045A pattern generator, 1 channel	M8057A		
Analyzer module, 32/64 Gbaud, 1-slot AXIe	**M8046A**		
Analyzer, one channel, data rate up to 32 Gbaud, NRZ	M8046A	A32	
Analyzer, one channel, data rate up to 64 Gbaud, NRZ	M8046A	A64	
Equalization, license (only needed for > 32 Gbaud)	M8046A	0A3	Only with A64
PAM4 decoding up to 32 Gbaud, license	M8046A	0P3	
Clock recovery for 32 Gbaud, license	M8046A	0A4	
Clock recovery extension to 64 Gbaud, license	M8046A	0A5	Only with A64 and 0A4
Interactive link training for PCIe, license	M8046A	0S1	Requires 0A4, 0G4
SKP OS filtering for PCIe and CCIX, license	M8046A	0S2	
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input	M8046A	801	Qty 1 recommended
Matched cable pair 2.4 mm(m) to 2.4 mm (m)	M8046A	002	Qty 1 recommended
Software and chassis			
System software for M8000 Series	M8070B	unlicensed	
Advanced measurement package	M8070ADVB	1FP/1TP/ 1NP/1UP [1]	
Error distribution analysis package	M8070EDAB	1FP/1TP/ 1NP/1UP [1]	
5-slot AXIe chassis with USB option	M8040A	BU2	
5-slot AXIe chassis with USB option and embedded controller M9537A	M8040A	BU1	
Warranty, calibration and productivity services			**see next page**

1. Multiple types of licenses are available. Choose between 6/12/24 month support subscriptions.

Figure 23. Overview of possible M8040A configurations

Description	Product #	Option	Comment
Upgrades for M8040A High-performance BERT 64 Gbaud	M8040AU		
Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe	**M8045A**		
Upgrade to 64 Gbaud	M8045A	U64	License
Upgrade to second channel, hardware and license (requires remote head, M8057A)	M8045A	UG2	Requires return-to-factory
Upgrade to advanced jitter sources for receiver characterization, module-wide license	M8045A	UG3	License
Upgrade to de-emphasis, module-wide license	M8045A	UG4	License
Upgrade to Forward Error Correction (FEC) encoding, module-wide license	M8045A	UG9	License
Upgrade to PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	UP3	License
Upgrade to extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	UP6	Only with G64/U64
Remote head for M8045A pattern generator, 1 channel	M8057A		
Analyzer module, 32/64 Gbaud, 1-slot AXIe	**M8046A**		
Upgrade M8046A for data rates up to 64 Gbaud, NRZ	M8046A	U64	Requires return-to-factory
Upgrade to equalization, license	M8046A	UA3	Only with A64/U64
Upgrade to PAM4 decoding up to 32 Gbaud, license	M8046A	UP3	License
Upgrade to clock recovery 32 Gbaud, license	M8046A	UA4	Requires return to factory for S/N<DExxx01000
Upgrade to clock recovery extension to 64 Gbaud, license	M8046A	UA5	Only with A64/U64
Upgrade to interactive link training, license	M8046A	US1	Requires return to factory for S/N<DExxx01000
Upgrade to SKP OS filtering for PCIe and CCIX, license	M8046A	US2	License

Figure 24. All upgrade options for M8040A are orderable under M8040AU. Most options are license options, that can be upgraded on site.

Default accessories included with shipment

M8045A module: Four 50 Ω resistors, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables, no blue sync cable
M8046A module: One bandpass filter for clock input, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables
M8057A remote head: includes cable connection to M8045A pattern generator module, one 50 Ω termination (2.4 mm)
M8040A-BU1: M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord
M8040A-BU2: M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord
M8070B: CD-ROM with M8070B system software

Recommended accessories

Short cable, 1.85 mm (m) to 1.85 mm (m), 0.15 m, 699 ps delay ± 1 ps (two are recommended for each differential data output of M8057A)	M8045A-801
Matched cable pair 2.4 mm (m) to 2.4 mm (m), 2 ps, length 0.85 m (recommended for data input of M8046A analyzer)	M8046A-802
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m (recommended for clock input of M8046A analyzer)	M8046A-801
M8000 sync cable (when using the system clock of M8045A for M8046A) and LINK 1234 connection	M8051A-801
Attenuator, 6 dB, 1.85 mm	8490G-006
DC block 2.4 mm	N9398F
Matched directional coupler pair 50 GHz, 13 dB, 2.4 mm (recommended for external interference source RI/SI)	M8045A-802
Matched coupler pair 40 GHz, 12 dB, 2.4 mm	M8045A-803
Bandpass filter 11.1 to 17.5 GHz, SMA (for M8046A clock input)	M8061A-803
Microwave pick-off tees, 2.4 mm, matched pair (Qty 1 is recommend for use with N1076A/77A)	N1027A-2P2
Microwave pick-off tees, 1.85 mm, matched pair (Qty 1 is recommend for use with N1076B/N1078A up to 32 Gbaud)	N1027A-2P8
Microwave pick-off tees, 1.0 mm, matched pair (Qty 1 is recommended for use with N1076B/N1078A above 32 Gbaud)	N1027A-2P1
Adapter 1.0 mm (m) to 1.85 mm (m) (Qty 2 is recommended for use with pick-off tees N1027A-2P1)	11921G
Adapter 1.0 mm (f) to 1.85 mm(f) (Qty 2 is recommended for connecting data cables to pick-off tee N1027A-2P1)	11921F
Adapter 2.4 mm (f) to 2.4 mm (f) (Qty 2 is recommended for connecting cables to pick-off tees)	11900B
Adapter 3.5 mm (m) to 3.5 mm (m) (Qty 2 is recommended for connecting pick-off tees directly to N1076A/77A inputs)	83059A
Rack-mount kit for AXIe 5-slot chassis M9505A	Y1226A

Calibration, warranty, and productivity services

Calibration services (3 and 5 years)	R1282 (R-50C-011-3/-5)
Warranty extension to 3/5 years	R1280
Productivity assistance	R1380-M8000

Related Keysight Literature

Data sheets

J-BERT M8020A - Data Sheet	5991-3647EN
M8030A Multi-channel BERT - Data Sheet	5992-1287EN
M8062A 32 Gb/s Front-end - Data Sheet	5992-0987EN
M9505A AXIe Chassis 5-slot - Data Sheet	5990-6584EN
M8196A 92 GSa/s AWG - Data Sheet	5992-0971EN
N1085A PAM4 Measurement Application for 86100D DCA-X Series - Data Sheet	5992-1248EN
N1076A/N1076B/N1077A/N1078A Clock recovery - Data Sheet	5992-1620EN
N4917BSCA Optical Receiver Stress Test Solution IEEE 802.3bs - Data Sheet	5992-2554EN
M8049A ISI Channel Boards - Data Sheet	5992-3617EN
M8091BSPA IEEE802.3bs Receiver Test Pre-Compliance Application - Data Sheet	5992-3288EN
M809256PA OIF-CEI-56G Receiver Test Application - Data Sheet	5992-3292EN

Application notes, white papers and posters

Characterizing and verifying compliance of 100Gb Ethernet components and systems - Application Note	5992-0019EN
Master 400G - Poster	5992-2143EN
Equalization: The correction and analysis of degraded signals - White Paper	5989-3777EN
BER measurement using a real-time Oscilloscope controlled from M8070A system software - Application Note	5992-2676EN
Advanced modulation and coding challenges - White Paper	5992-3021EN
Error analysis of PAM4 signals - Application Note	5991-3724EN

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