DDR3 DIMM 1867 Interposer

For use with Agilent Logic Analyzers

FuturePlus® Systems

Power Tools for Bus Analysis

- **DDR3 1867 MT/s bus analysis**
- **Supports Agilent 16900-series logic analyzers**
- **Includes protocol-decode software, probe configuration software, and automatic logic analyzer configuration software**
- **Optional Protocol Compliance and Analysis software available**
- **Interposer design does not consume a slot**
- **Now includes Clock Qualifier feature to allow accurate testing in 2 rank systems (NEW)**

FS2352 DDR3 DIMM 1867 Interposer

Key Features

- Quick and easy connection between the DDR3 DIMM SDRAM memory bus connector and Agilent logic analyzers
- Complete and accurate 1867 MT/s state analysis or timing analysis up to 8 GHz
- Compatible with all 240-pin DDR3 SDRAM DIMM's up to 1867 MT/s.
- All signals are probed passively.
- Does not require termination adapters; they are built-in
- Registered and non-registered DIMMs are supported.
- Burst sizes of 2, 4, or 8 are supported.
- Monitors writes only, reads only, or writes and reads.
- Read and write burst type is tracked and each cycle of a burst (in both state and timing mode) is flagged by the analyzer as a read or write

Straightforward, Reliable DDR3 1867 Analysis

The FuturePlus FS2352 DDR3 DIMM 1867 Interposer provides a mechanical, electrical and software interface between an Agilent logic analyzer and the DDR3 1867 connector. The FS2352 is used to design and debug computer motherboards and DIMM's incorporating DDR3 1867 technology.

Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our Interposers and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

Agilent Technologies

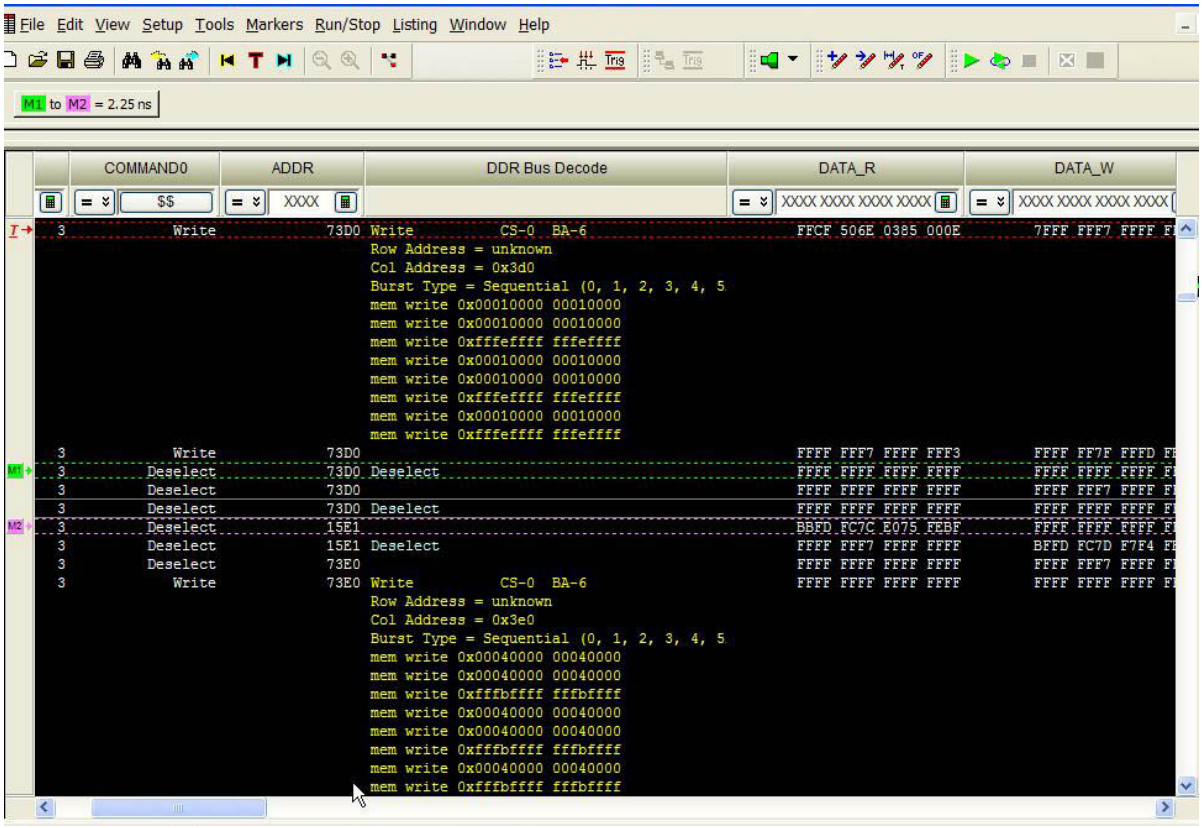
Solution Partner

Since 1991

Accurate State Analysis

The FS2352 DDR3 1867 DIMM memory bus interposer brings bus signals to your Agilent logic analyzer via controlled impedance cables for an easy protocol analysis connection while maintaining signal fidelity.

Protocol Analysis



The FS2352 protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features. Depending on the logic analyzer's resources, the FS2352 interposer can be configured to perform State analysis of Reads or Writes, or both Reads and Writes, at 1867 MT/s.

The DDR protocol decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. User-selectable post-processing filters allow the acquired data to display different types of transactions indifferent colors.

What are the advantages of using an interposer?

More Powerful

- ❑No sacrifice of a slot like a V-DIMM
- ❑You can test a fully loaded bus with an interposer!

More Flexible

- ❑Allows the use of any DIMM from any vendor

Lower Cost

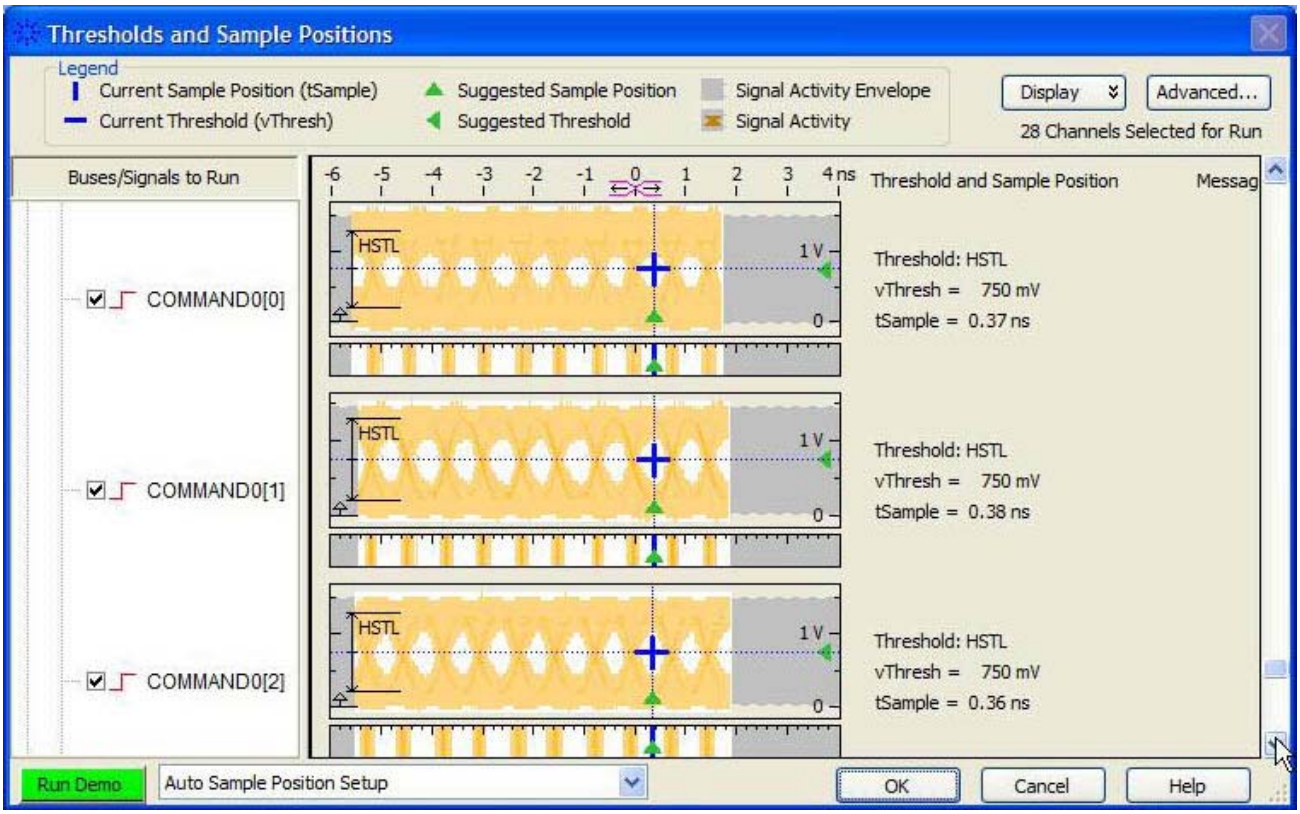
- ❑Interposer enables debugging of any DIMM configuration

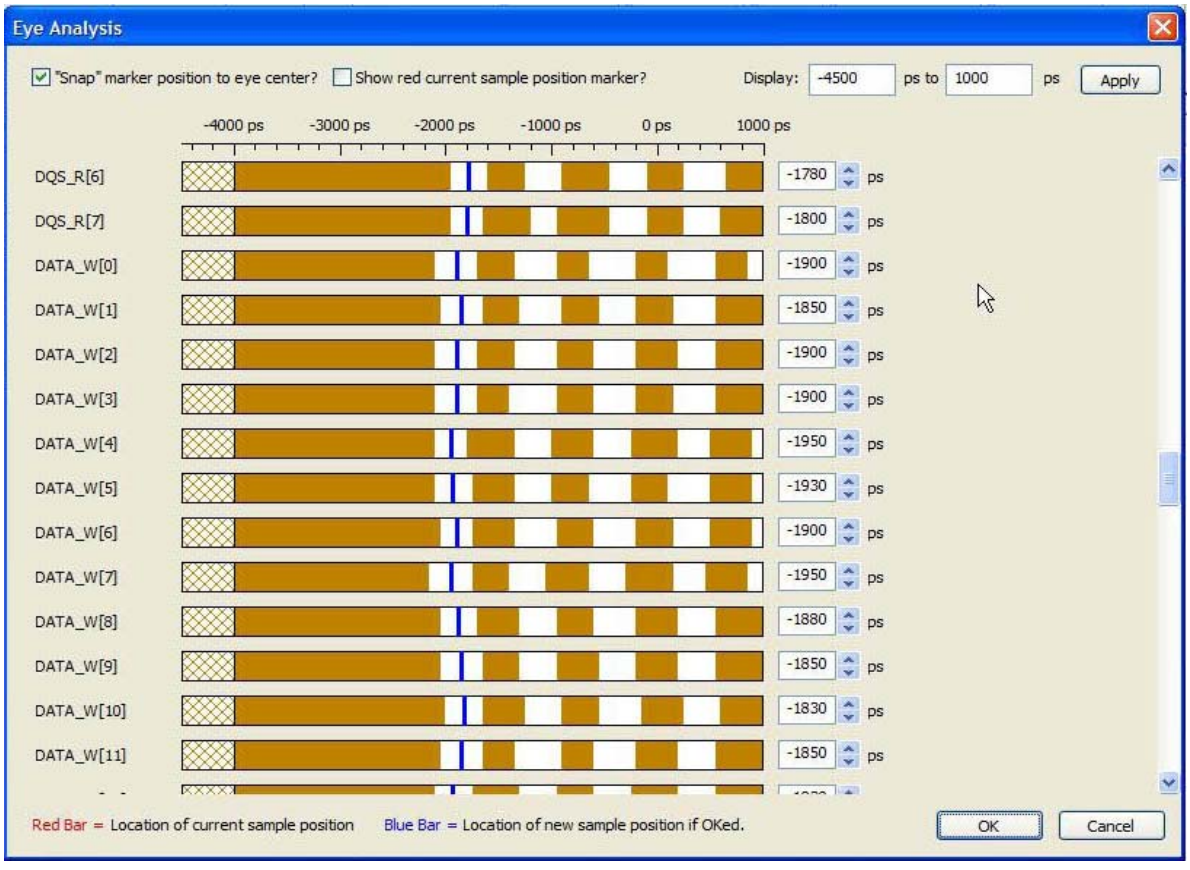
More reliable

- ❑Less components, no memory chips

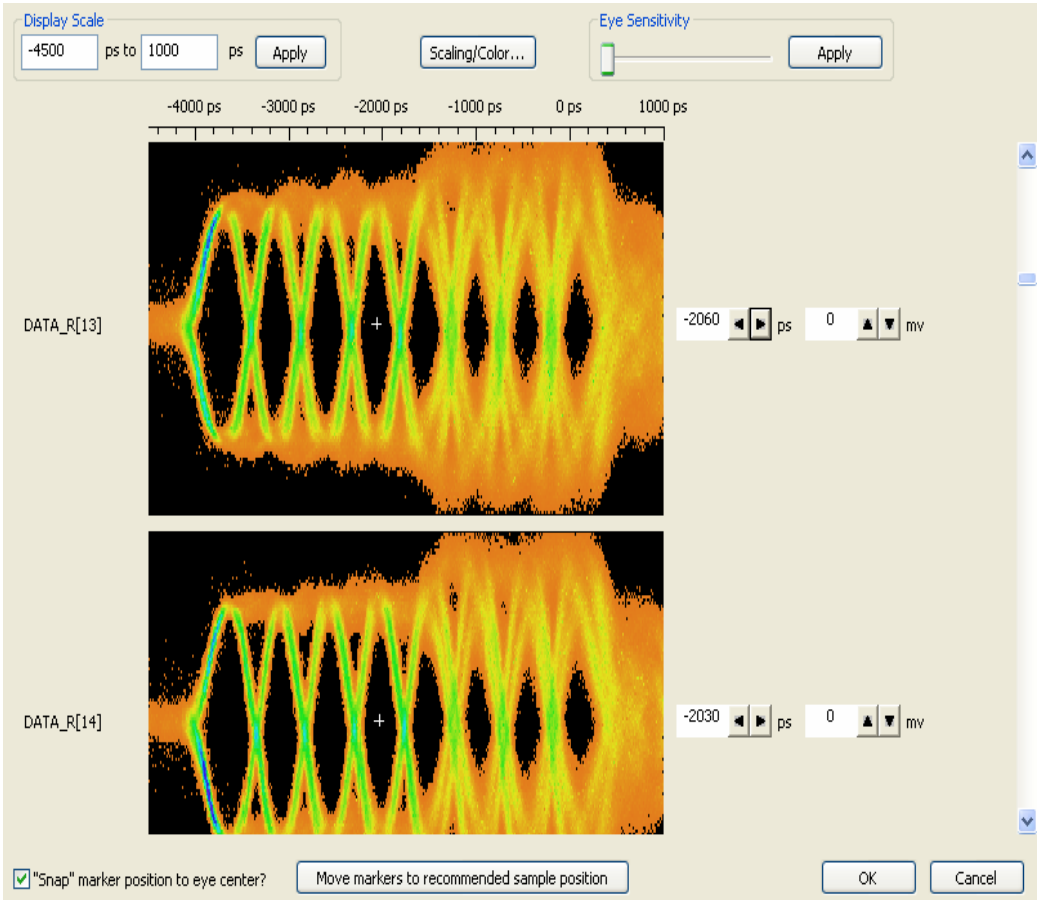
Signal Integrity Insight

Quickly gain signal integrity insight with Agilent EyeScan technology. As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement of the design verification process. EyeScan lets you quickly acquire comprehensive signal integrity information on the DDR3 bus in your design, and can provide measurements with 5 ps of resolution.

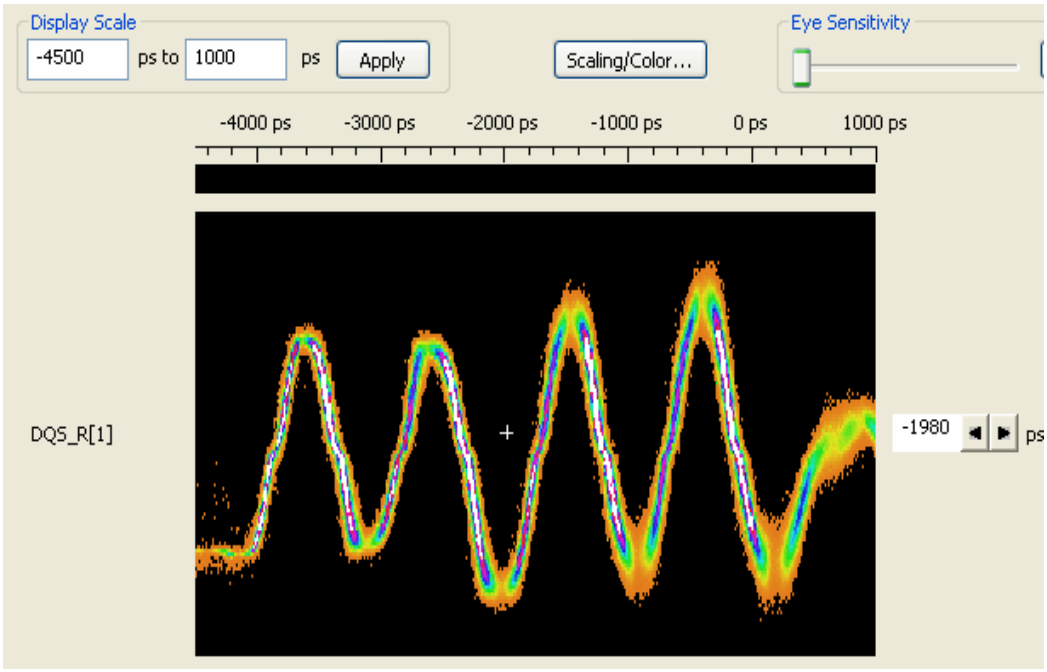




Excellent Signal Integrity during a 1R READ Burst MEMTest #7

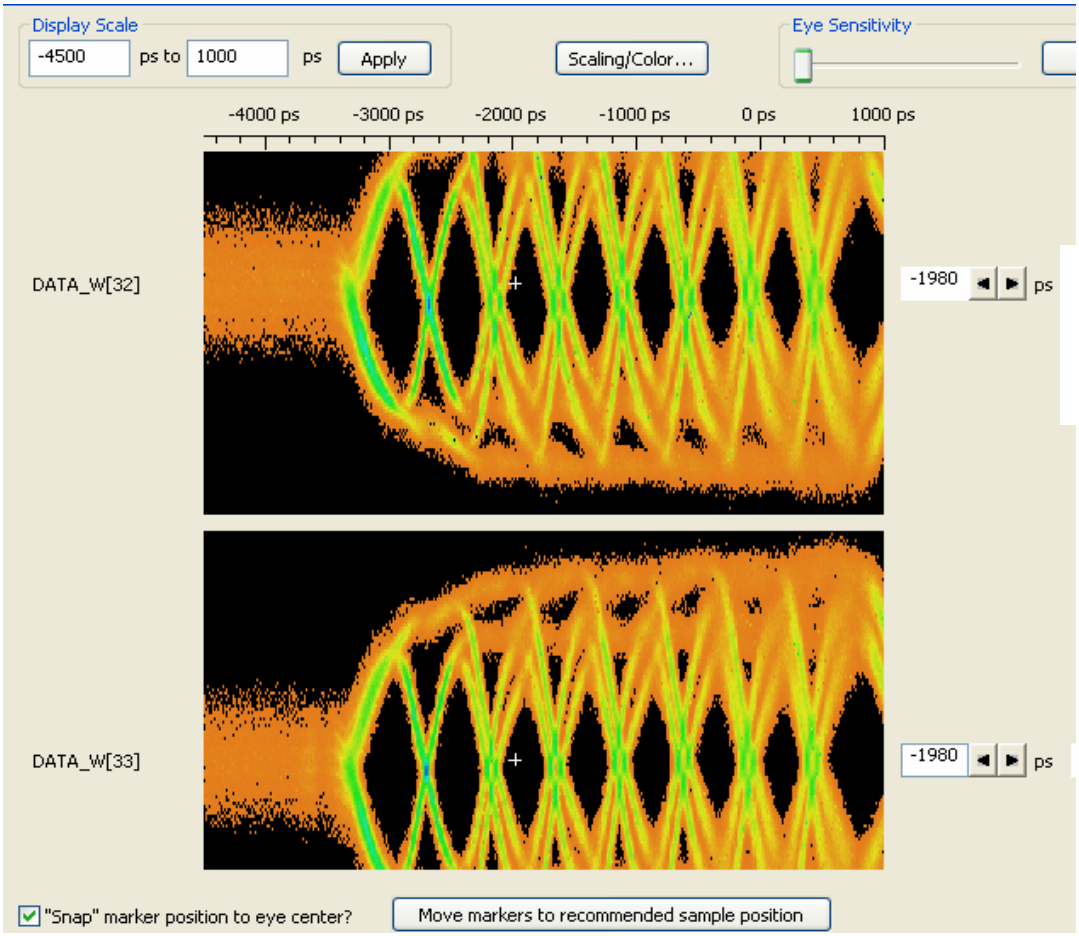


Note that the large eyes are 300 ps by 460 mv. The small eyes are 235 ps by 205 mv. The large eye during the first part of the burst changing to the smaller eye later is probably related to the MB controller overdriving the bus. Note the corresponding effect on the DQS1

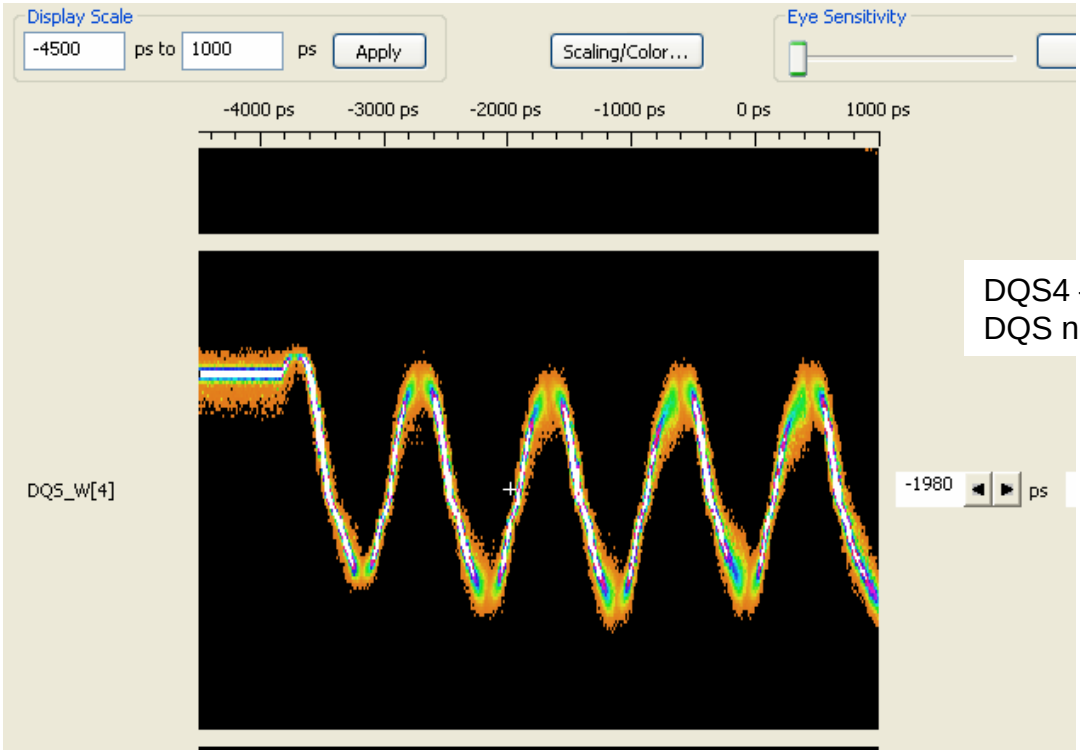


Note the effect on the DQS1 during the last half of the burst. It seems to be overdriven which results in amplitude jitter. This matches what we see on it's corresponding Data bits.

Excellent Signal Integrity during an 1867 1R WRITE Burst MemTest #7



Note the large eyes are 315 ps by 445 mv. The small eyes are 260 ps by 360 mv. There seems to be some non-random Clock to Data bit jitter here. The DQS bit does not show much jitter.



DQS4 – no noticeable Clock to DQS non-random jitter

Ordering Information

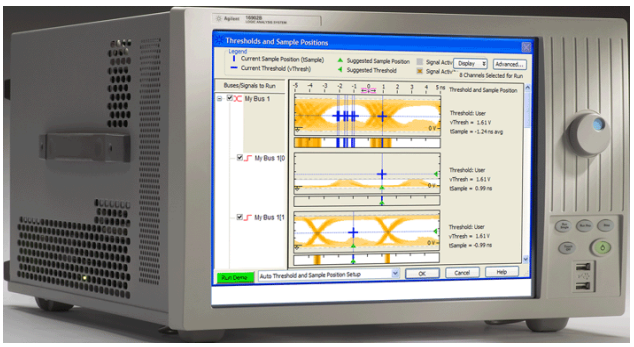
FS2352 – DDR3 1867 Interposer for use with Agilent Logic Analyzers

Software included with the FS2352:
Configuration files for the Agilent logic analyzer
Protocol Decoder software, runs on the Agilent logic analyzer

Optional Software Available from Agilent Technologies:
B4622A DDR3 Protocol Compliance and Analysis Tool

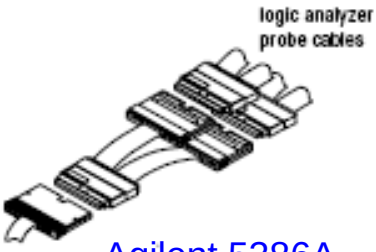
Agilent Logic Analyzer Requirements

The FS2352 requires:
- 1 ea 16902B Modular Logic Analysis System
- 4 ea 16962A 68-Channel, 2 GHz State Logic Analyzer Modules
- Up to 1 ea E5386A half channel probe adapter per 16962A for 8 GHz timing analysis



Agilent 16902B

Agilent 16962A



Agilent 5386A

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