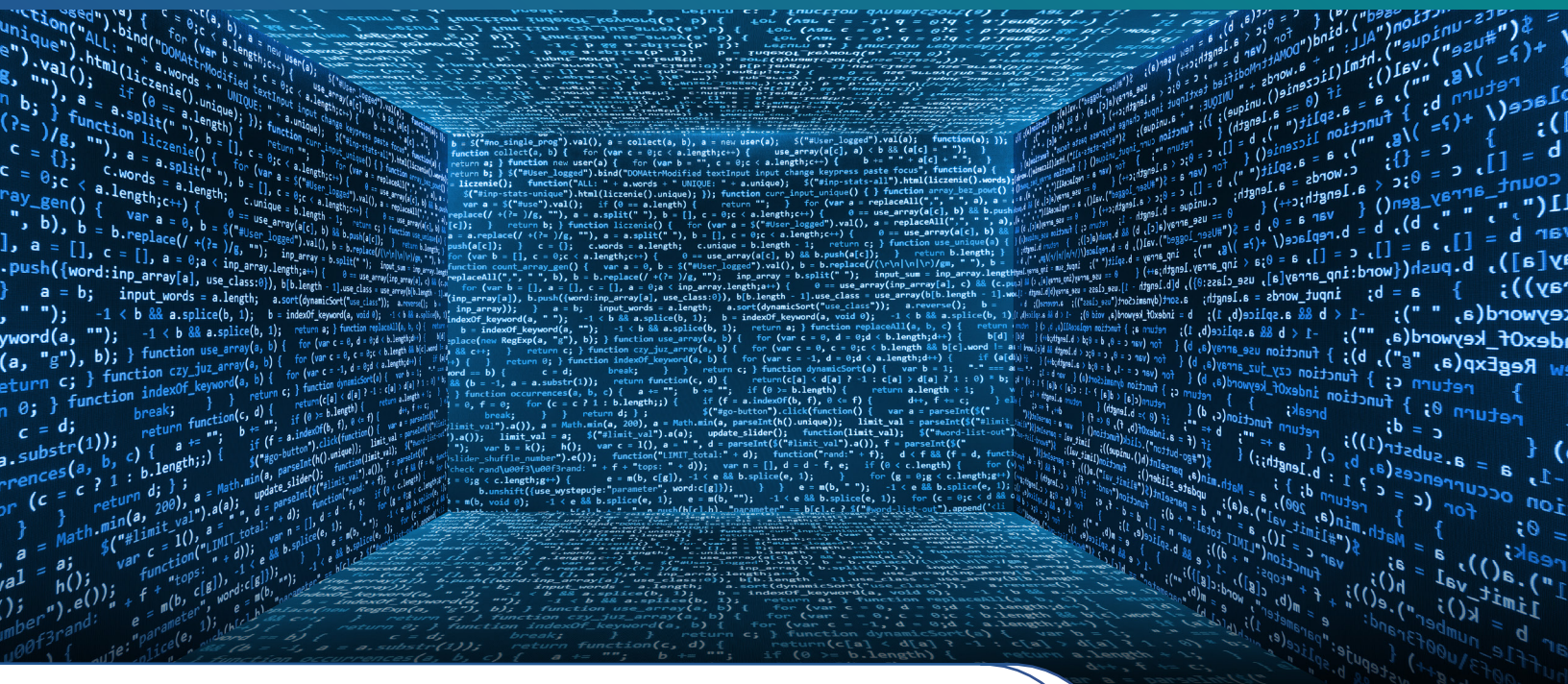

WHITE PAPER

BERT Applications Fundamentals Series

Computer bus and communications interface data rates continue to increase while transmission margins shrink. This drives the need for equalization techniques in transmitters and receivers to compensate for the lossy channels. Electrical signal degradations are caused by printed circuit boards or cables between the serial transmitter and the receiver interface ports. Picking the bit error rate tester (BERT) for your application can be a costly and time-consuming effort. Follow these application hints to reduce your selection time.

High-Speed Applications

Your device type, bit rate, and digital interface will drive the BERT solution that fits your application. Refer to Table 1 below for a shortcut to your solution.

Device	Bit rate	Application examples	Typical requirements
High-speed serial receiver in computer buses and backplanes	< 16G	QPI, PCI Express, SATA, SAS, USB3, TBT, DP, SD, UHS II, MIPI D-PHY/M-PHY, HDMI	Data rates < 16 Gb/s, calibrated jitter, SSC, ISI and S.I., clock recovery, pattern sequencing
	< 10G	MIPI D-PHY/C-PHY, HDMI, MHL	Data rates < 10G, no loopback, 3-wire or multi-level
Backplanes, cables, SERDES, AOC, Repeaters	> 10G to 28G	10GBase-KR4/-CR4, CEI, IB, TBT, CAUI, CAUI 2/4, 10Gbase-KR	Data rates > 10 Gb/s, de-emphasis, x-talk, PRBS
	< 58G	CEI-56G/112G, 400 GbE	PAM-4, NRZ, PRBS
Optical transceivers and sub-components: 0.6 to 58 Gb/s	< 58G	400 GbE, 64G FC	PAM-4, NRZ, PRBS
	< 28G	40G/100 GbE, 32G FC, CFP2/4	Data rates > 16 Gb/s clean signals, PRBS
	10G	10G/40 GbE, PON, OTN, 8G/16G FC, QSFP, SFP+, QFP	Data rates 3 to 15 Gb/s, PRBS optical stress and sensitivity, framed bursts

Table 1: High-speed digital interfaces

KEYSIGHT TECHNOLOGIES

What follows are some of the more common BERT applications.

Interactive Link Training

PCI Express, storage interfaces, and backplane standards require link partners to optimize the TX de-emphasis and RX equalization combination. This requires your transmitter to change its de-emphasis as requested from your receiver. In order to perform these tasks, your BERT must be able to understand low level protocol and react to the commands. Basically, your BERT needs to behave like a link partner in your system and help you interactively perform link training, reacting to both equalization and de-emphasis requests.

Emulate De-Emphasis and Compensate for Channel Loss

This is common when operating above 5 Gb/s. Both R&D and test engineers need to characterize receiver ports under realistic and worst-case conditions. So your BERT must provide a pattern generator signal that will accurately emulate transmitter de-emphasis and have an adjustable number of tap levels.

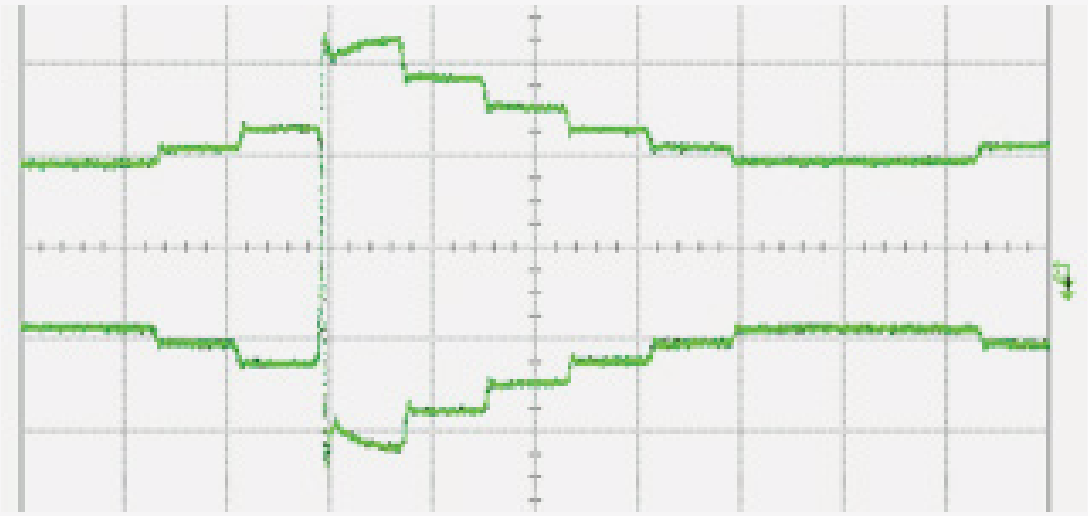

Figure 2: An example of a BERT output with eight tap levels

Emulate Channel Loss with Integrated and Adjustable ISI

With increasing data rates, your channel loss between transmitter and receiver in digital designs becomes extremely important. This channel loss results in what is called intersymbol interference (ISI) and consists of time jitter and amplitude interference. Your ISI levels are affected by the channel material, dimensions, the data rate, and the bit pattern. High-speed digital receivers are specified to tolerate a certain amount of ISI loss. You will want your BERT to provide integrated and adjustable ISI to emulate channel loss during your receiver characterization. Another robust BERT feature offers adjustable and independent ISI levels on each channel.

NRZ and PAM-4 Signals Operating Up to 32 and 64 Gbaud Require Accurate Receiver Characterization

You will need integrated jitter sources and de-emphasis capabilities in your BERT to emulate the transmitter (TX) and to simulate channel loss in your test setup. It is also helpful to have a BERT that will emulate an aggressor lane. To do this, your BERT will need an internal clock synthesizer and a second pattern generator output channel. A BERT that integrates transmitter, receiver, and test set-up connections makes your job easier. It will make your test results more robust, calibration simpler, and the frequency of re-adjustments reduced, resulting in a more efficient use of your overall test time.

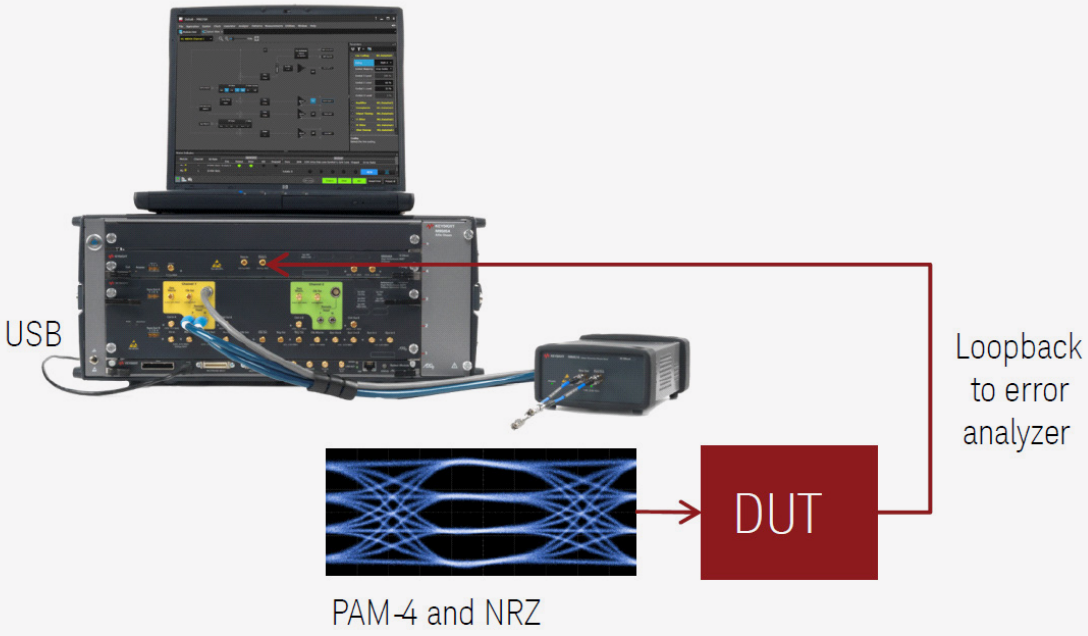

Figure 3: The Keysight M8040A streamlines complex receiver test setups

Each of the one or two pattern generator channels in Figure 3 provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real-time for NRZ and PAM-4 signals without the need to split up the PAM-4 signal for multiple error detector channels.

Input Tolerance Testing

You may need more than one BERT channel so one can be used as an aggressor lane to emulate crosstalk effects. Look for a BERT with adjustable data rates and several pattern standards as well as jitter functions. For additional channel stress you will need a BERT to emulate transmitter de-emphasis and compensate for loss in the test setup. Random interference (RI) and sinusoidal interference (SI) options with software control on source and aggressor lanes are a plus. And lastly, the BERT should have several automated tolerance test capabilities.

PAM-4 and NRZ Receiver Test Challenges

Signal integrity issues with 25 Gb/s NRZ and PAM-4 device testing pose a challenge to design and test engineers who need to characterize their devices. Impairments that may occur in the real-world should be tolerated by the receiver under test without exceeding the desired BER level. For example, a typical input receiver tolerance test should include jitter tolerance, interference tolerance test, and level sensitivity margins that are applicable for NRZ and PAM-4 devices. In addition, PAM-4 receivers require additional margin testing for level non-linearity, cross-talk effects from adjacent lanes, and vertical eye closure. Figure 4 shows this level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

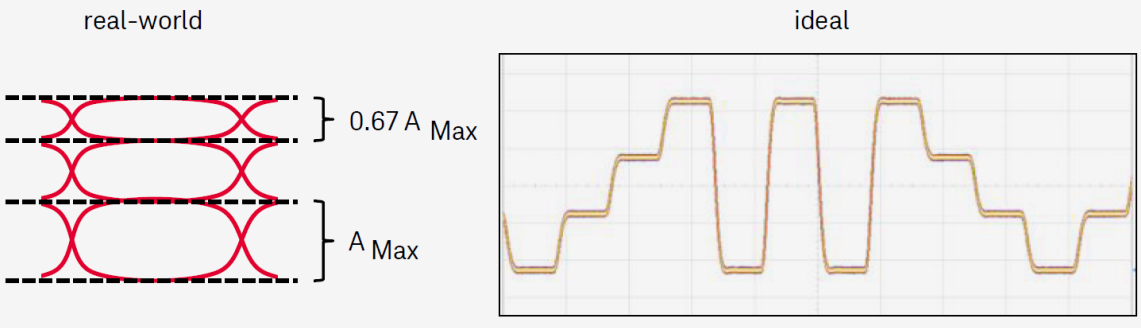

Figure 4: PAM-4 eyes can show a level separation mismatch

Real-Time Error Analysis for PAM-4 Signals

Receiver verification checks whether the receiver under test operates below the specified BER while emulating worst-case transmitter and channel conditions. For proper error detection of PAM-4 signals, all voltage thresholds need to be analyzed simultaneously to ensure a correct symbol error measurement. (See Figure 4 above.) For example, if a “1“ is detected at the mid-voltage threshold, the received pattern can have level two or three The peak-to-peak level must be checked simultaneously to determine if the received inputs have the correct level for a two or a three. If the two thresholds are in error within one-unit interval, an error is created.

Receiver Interconnect Standards

Communication standards are changing every year. You should check to see that your BERT can provide the following to ensure you can test symbol rates up to 32 and 64 GBaud:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- OIF CEI - 56G (NRZ and PAM-4 versions)
- 64G/112G Fibre Channel
- Infiniband-HDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

Suggested Reading and Sources

Make an informed decision when purchasing your next BERT. Know more than just your BERT characteristic and specifications. Understand how your specific application drives the BERT capabilities you need to successfully test your system under real-world conditions. Whether it is in R&D, characterization, QA, compliance testing or manufacturing test, Keysight has the BERT to fit your needs. To learn more about Keysight's BERT options, **click here**.

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

KEYSIGHT TECHNOLOGIES