TELEDYNE LECROY
Everywhereyoulook™

Compute Express Link® (CXL®) Protocol Analysis

Key Features

Find errors fast

- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic

- Get useful information
- More choices of data views
- More ways to analyze data
- Custom decoding and reports

Data capture

- 100% data capture up to 64.0 GT/s

Supported platforms

CXL is offered as an optional feature on the following Teledyne LeCroy PCIe® protocol analyzers and/or exercisers:

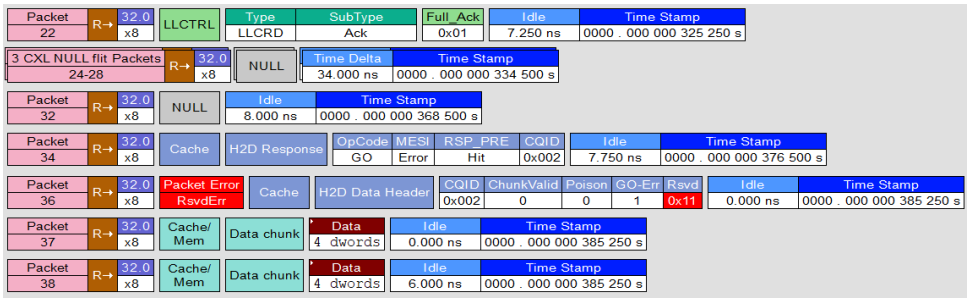
- Summit M616 PCI Express Analyzer/Exerciser
- Summit T516 PCI Express Analyzer
- Summit Z516 PCI Express Exerciser
- Summit T54 PCI Express Analyzer
- Summit M5x PCI Express Analyzer/ Jammer

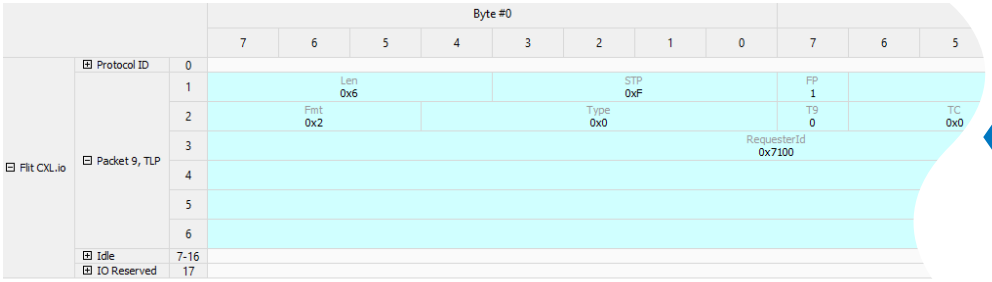
Compute Express Link (CXL) is a new high-speed CPU-to-Device and CPU-to-Memory interconnect designed to accelerate next-generation data center performance. CXL is based on the PCI Express® Physical layer with speeds up to 64GT/s. CXL technology maintains memory coherency between the CPU memory space and memory on attached devices, which allows resource sharing for higher performance, reduced software stack complexity, and lower overall system cost. This technology enables system operations to focus on target workloads as opposed to the redundant memory management hardware in their accelerators.

Teledyne LeCroy protocol tools can exercise, emulate, capture, decode, monitor and verify all of the various operations on the CXL link. Firmware and driver developers can use this test equipment to support development, debug, verification and validation of both PCIe and CXL devices. The CXL standard defines three protocols that are dynamically multiplexed together: CXL.io, CXL.cache, and CXL.mem.

By showing the transported flit through the entire link and transaction layers on the flex bus, these protocol analyzers are versatile to support protocol analysis at all layers from the FlexBus Physical layer and Flits all the way up to the Link and Transaction Layers. Protocol analyzers make use of the PCIe connectors for probing the DUT. These CXL protocol test solutions will provide the most useful decodes and various types of analysis and reports that help shorten development and testing time.

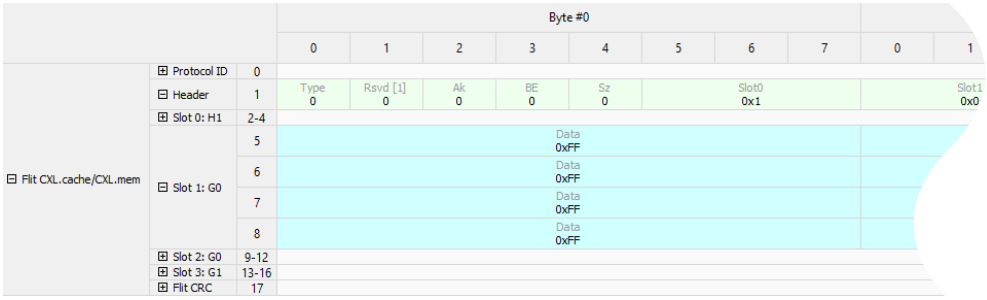
This trace shows a Link Layer Control Flit, and CXL.cache packets in a CXL Transaction. An error is indicated in Reserved field in the CXL.cache packet.

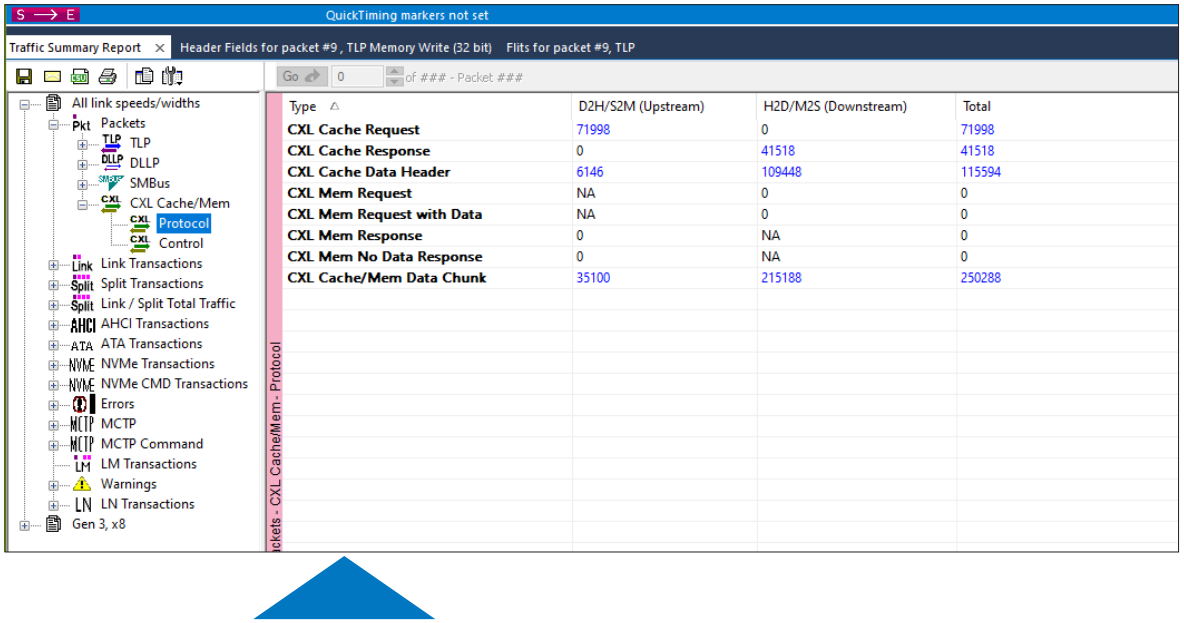




The Flit View from the CXL Trace shows a CXL.io Flit. Flits contain slots that carry one or more request/response messages or data chunks. The Flit header is also part of the slot.

The Flit View from the CXL Trace shows a CXL.cache/CXL.mem Flit. In this case, Flits contain slots that carry one or more request/response messages or data chunks.





Traffic Summary shows the CXL.io, CXL.cache and CXL.mem transactions upstream and downstream. Hyperlinked events bring you, with a single click, to the exact position in the trace where they occurred.

Ordering Information

Product Description	Product Code
Compute Express Link (CXL) Analysis option for Summit M616	PE6050SUA-A
Compute Express Link (CXL) Exerciser/Generation option for Summit M616	PE6070SUA-A
Compute Express Link (CXL) Analysis option for Summit T516	PE550SUA-A
Compute Express Link (CXL) Analysis option for Summit T54	PE391SUA-A
Compute Express Link (CXL) Analysis option for Summit M5x	PE392SUA-A
Compute Express Link (CXL) Exerciser/Generation option for Summit Z516	PE370SUA-A
CXL Compliance Test license for Summit Z516	PE376SUA-A
CXL Compliance Test license for Summit M616	PE6077SUA-A

Local sales offices are located throughout the world.
Visit our website to find the most convenient location.

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