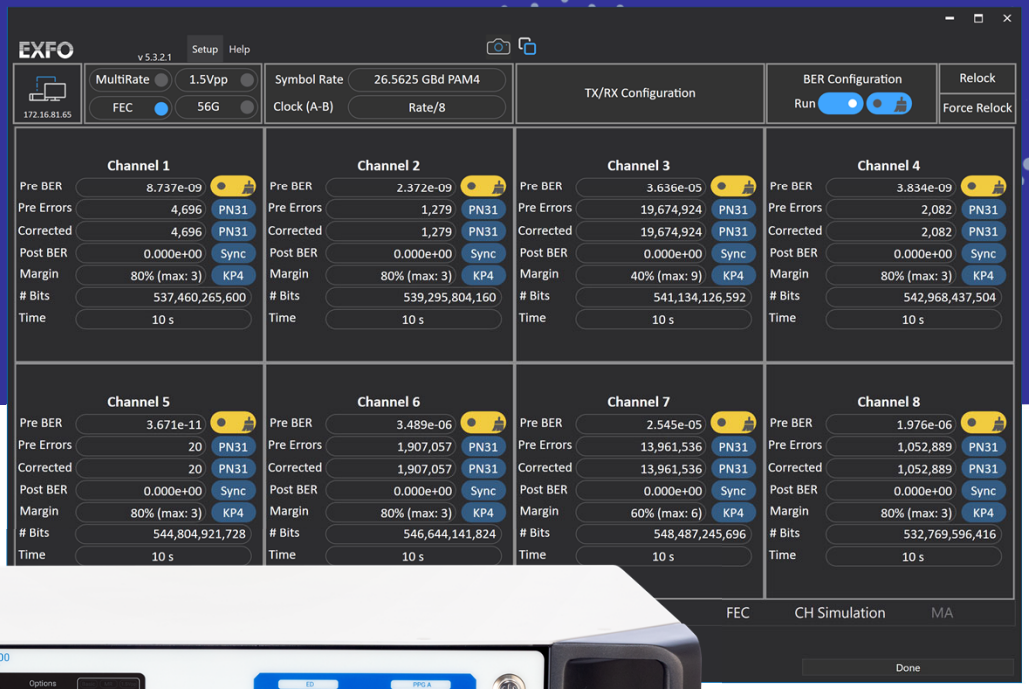
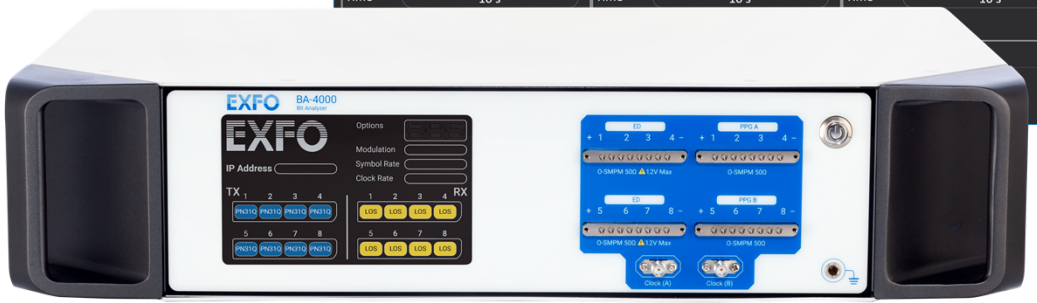
800G: Design and validation of new generation high-speed devices

EXFO BA-4000





Agenda

- Welcome and Introductions
  - Micah Hurd, TRS-RenTelco Product Manager
- EXFO: BA-4000 Technical Applications
  - Aldo Gutierrez, EXFO Business Development Manager
- EXFO/TRS-RenTelco Partnership: Equipment & Special Promotions
- Q&A – Joint TRS and EXFO

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80% of Calibrations Performed In-house

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Reliable Expertise

Strategic singular focus on the rental market

Top-tier rental partner to all major manufacturers

Financially Secure publicly traded company

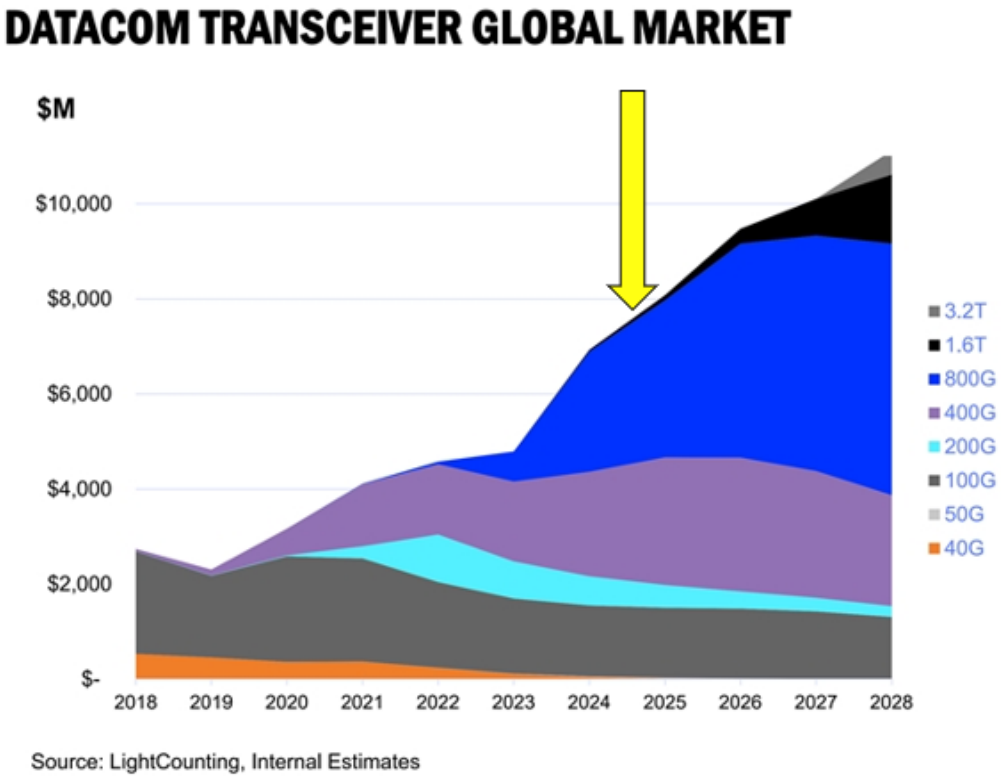
800G: Design and validation of new generation high-speed devices

Aldo Gutierrez
Business Development Manager

Agenda

- 800G Market review
- FEC: Technology Background
- BA-4000 for Advanced FEC
- Use Cases
- Key takeaways

Optical transceivers: forecast and trends

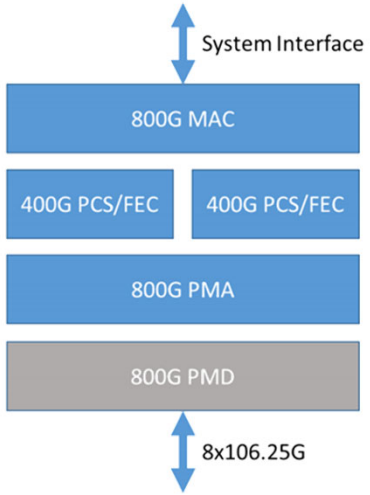


Source: LightCounting, Internal Estimates

Market timing

1. 800G (8x100G) optics up and running
2. 800G Ethernet (switch & router) now available
3. 800G (4x200G) expected in 2025

What is status for rates beyond 400G?



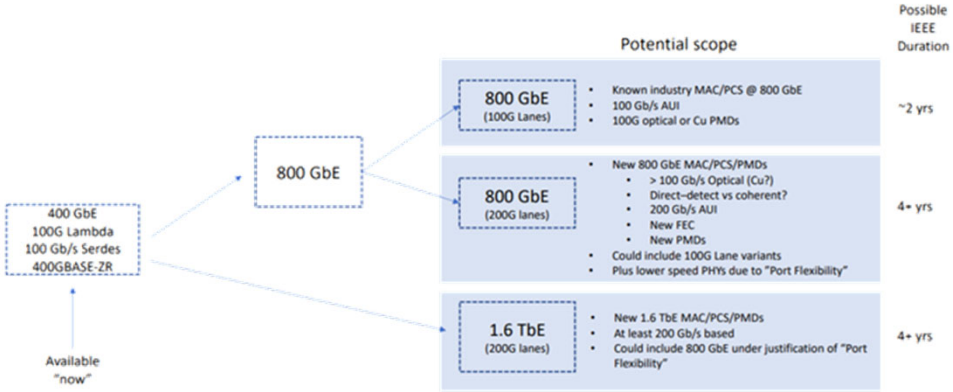
Ethernet Technology Consortium

ARISTA Microsoft Mellanox NVIDIA

BROADCOM Google

IEEE 802

IEEE 802.3 Beyond 400 Gb/s Ethernet Study Group

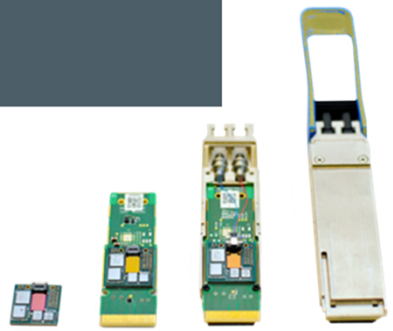


800G today's implementation: 8 x 53GBd PAM4

Road to 800G transceivers

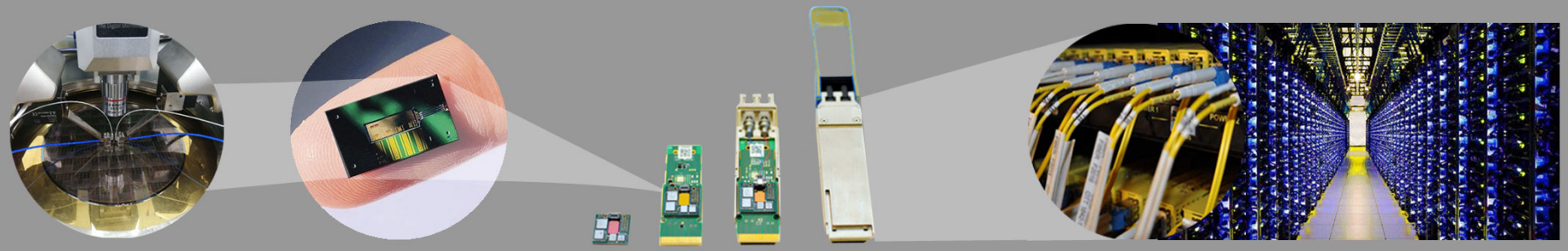
STRATEGIC MILESTONES

- Testing unframed PRBS on electrical lanes
- Advanced FEC for deep error analysis
- Testing with Layer-2 traffic
- Service turn-up in DC

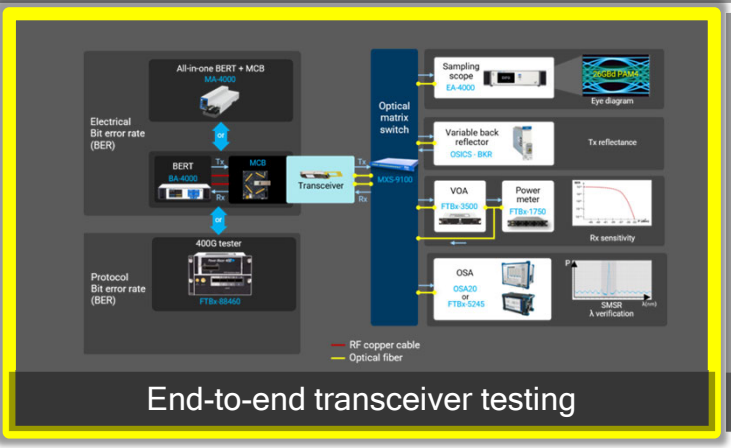


EXFO’s high speed testing ecosystem

Supports full ecosystem, from lab to field



Passive component and PIC testing



End-to-end transceiver testing

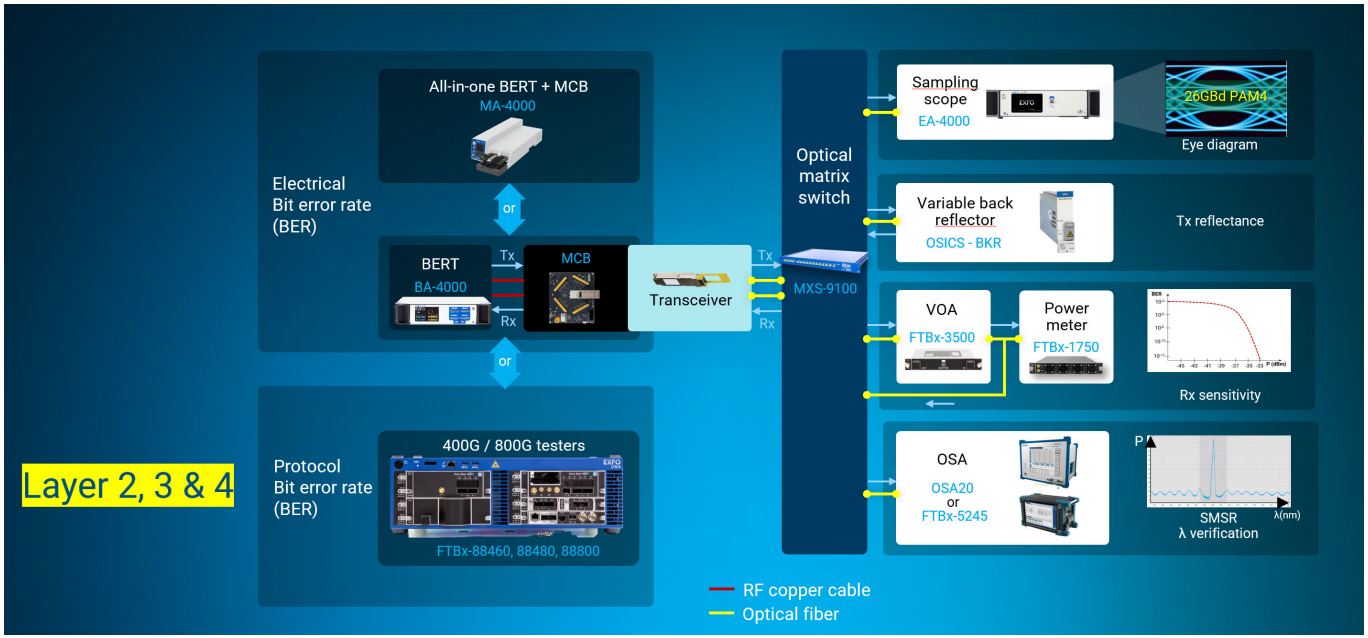
Transport and data center testing

EXFO's 1G-800G test solution: End-to-end transceiver tester

Complete optical, electrical and protocol testing for lab and manufacturing.

Efficient fast single-step validation on specs and industry standards.

Future-proof modular design supporting today's and tomorrow's optics and systems



EXFO's 800G test solution: from lab to tomorrow's manufacturing

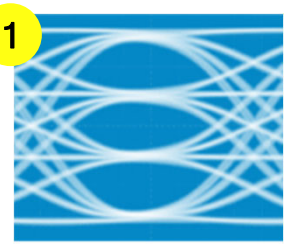
BA-4000: Physical-layer BER tester

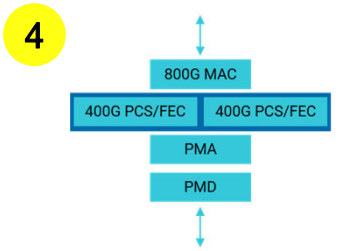
1. Supports 8 x 53 GBd PAM4
2. MCBs for new form factors
3. FEC & codeword analysis tools at 53G
4. Scrambled idle pattern complying the 800G draft standard

Enabler of 800G development

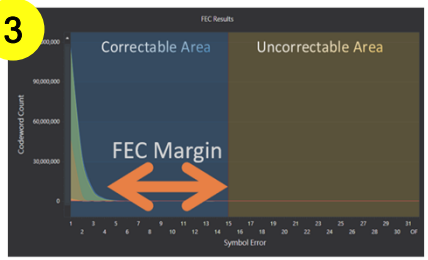
Highest signal integrity.

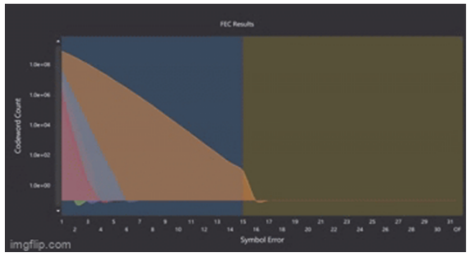
Advanced tools for optimized design.





800G BERT





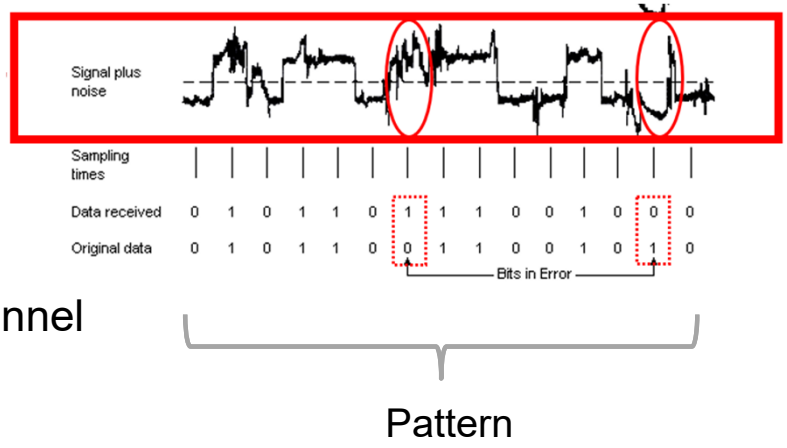
FEC: Technology Background

Why is PRBS testing not enough?

800 Gbit/s unframed PRBS testing is a good start to meet healthy BER but…

Limitation of unframed PRBS BERT

- Bit-error-rate test with PRBS will show errors within the pattern, but uncertain for instantaneous errors
- Burst errors are not well identified
- BER results are per channel only, which is fine for one channel testing validation but not realistic in context



Solution

Test BER with encoded FEC to analyze multiple channel integrity system for product design and validation

RS-FEC Scrambled Idle Pattern implementation based-on the ETC* 800G standard

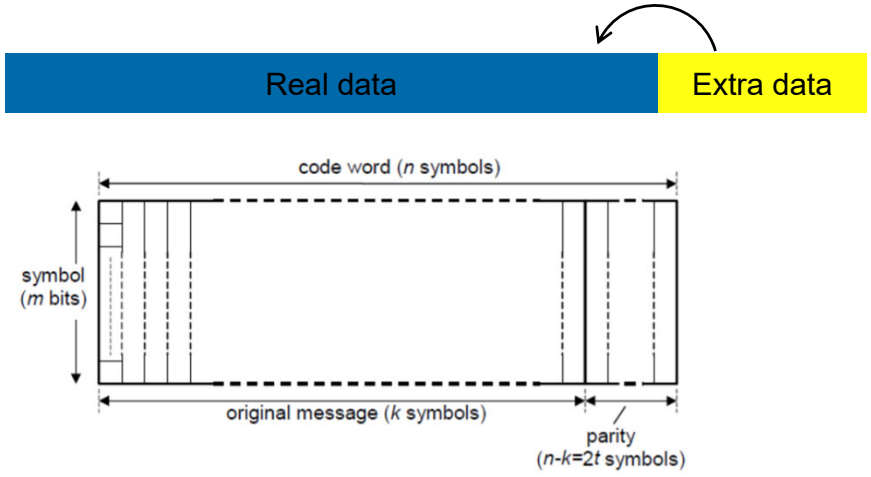
Forward error correction (FEC)

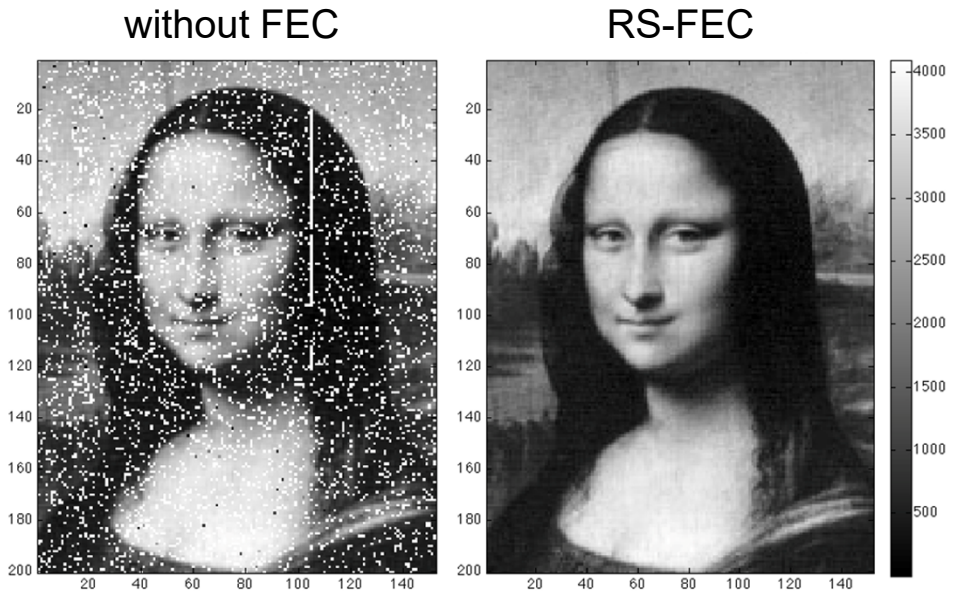
What is FEC?

It is an advanced coding technique that detects and autocorrects a certain number of errors through the links.

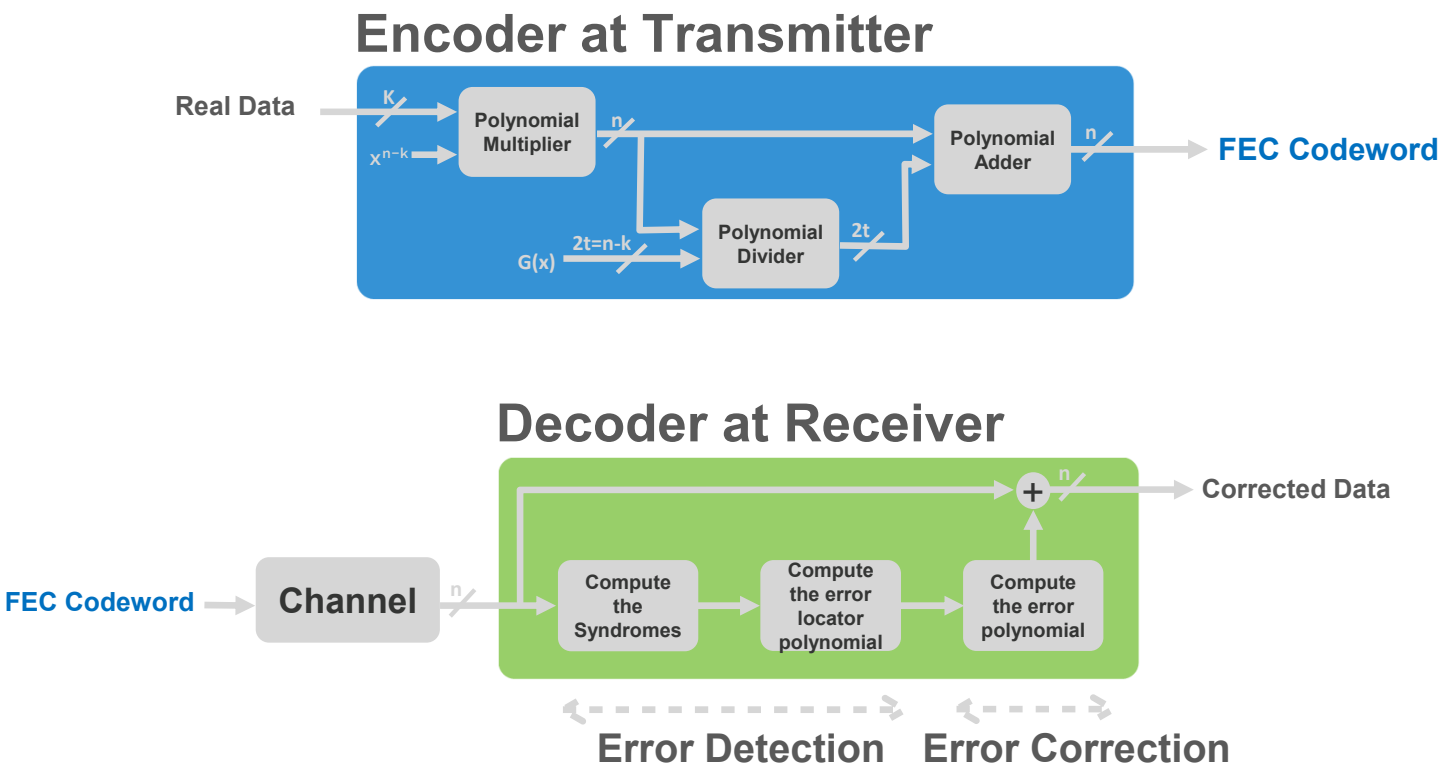
Principle of Reed-Solomon FEC (RS-FEC)

Extra data is added to the real data to protect it from getting corrupted.





Principle of FEC



FEC encoder adds extra data to protect real data on transmission side.

FEC decoder detects & corrects errors automatically on receiver side.

Why does FEC matter?

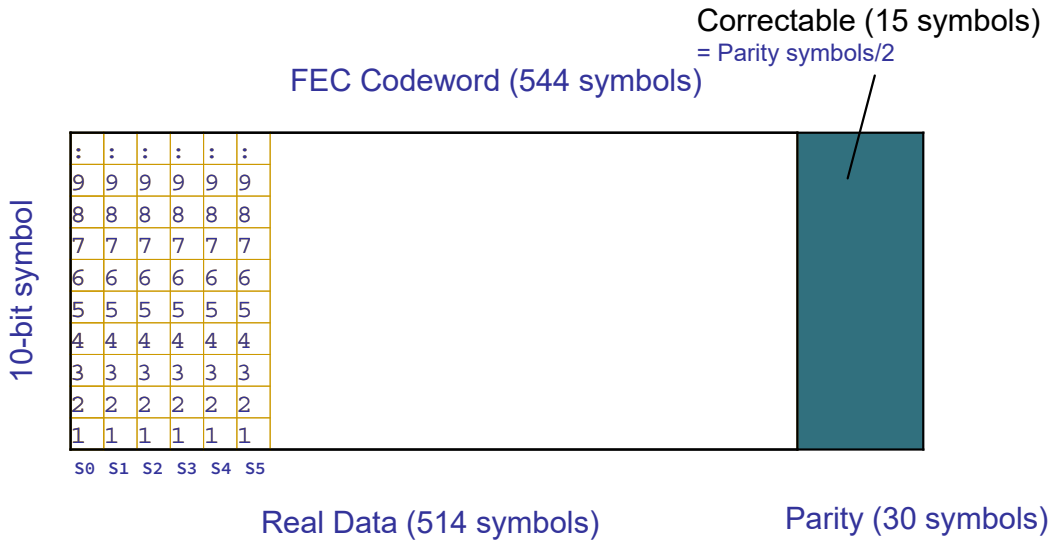
Why do we use FEC?
For 100G+ components, a healthy BER is not enough to guarantee transmission quality.
IEEE defined the FEC as mandatory in the specifications for 100G, 200G, 400G & 800G Ethernet.

Types of FEC
RS-FEC KR4: 100GBase-R
RS-FEC KP4: 400GBase-R, 800G Ethernet Technology Consortium
BCH: 800G FR4 pluggable MSA draft 1.0
CFEC: 400G ZR

Penalty
Increased latency, hardware complexity and power consumption.

RS-FEC KP4 technology

- RS-FEC KP4 is mainly used in 400GE and 800GE applications
- IEEE Beyond 400G study group is discussing to use KP4 in 800GE, 1.6TE



RS-FEC KP4 can correct up to 15 symbols in each FEC codeword.

RS-FEC KP4 correction mechanism

FEC can correct symbol errors ≤ 15

Cannot correct symbol errors > 15 →

Uncorrectable codewords → Frame loss

Random Errors

15 single bit errors in 15 symbols

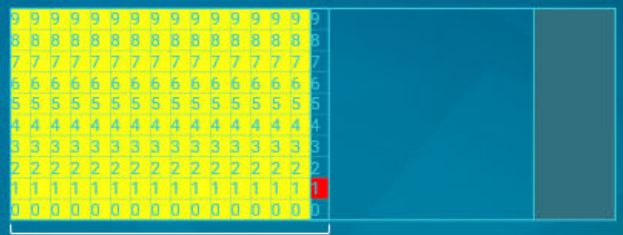
Long Burst Errors

150 bits burst errors in 15 symbols

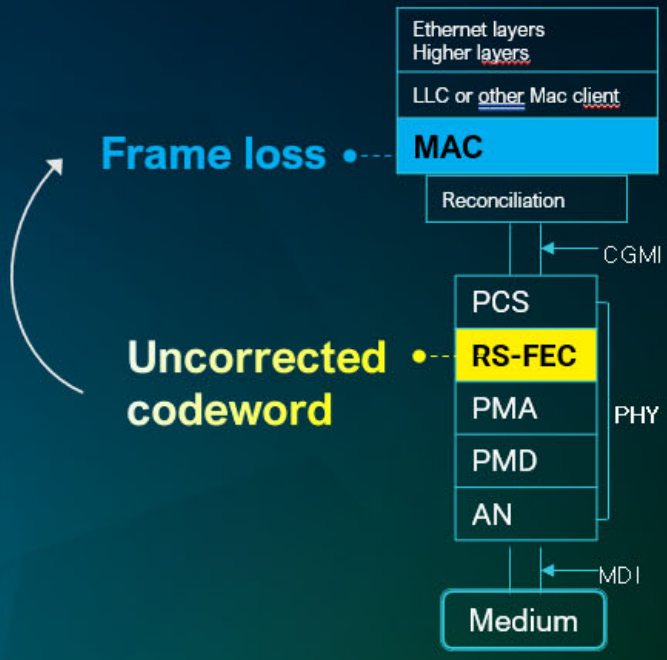
Longer Random Errors

16 single bit errors in 16 symbols

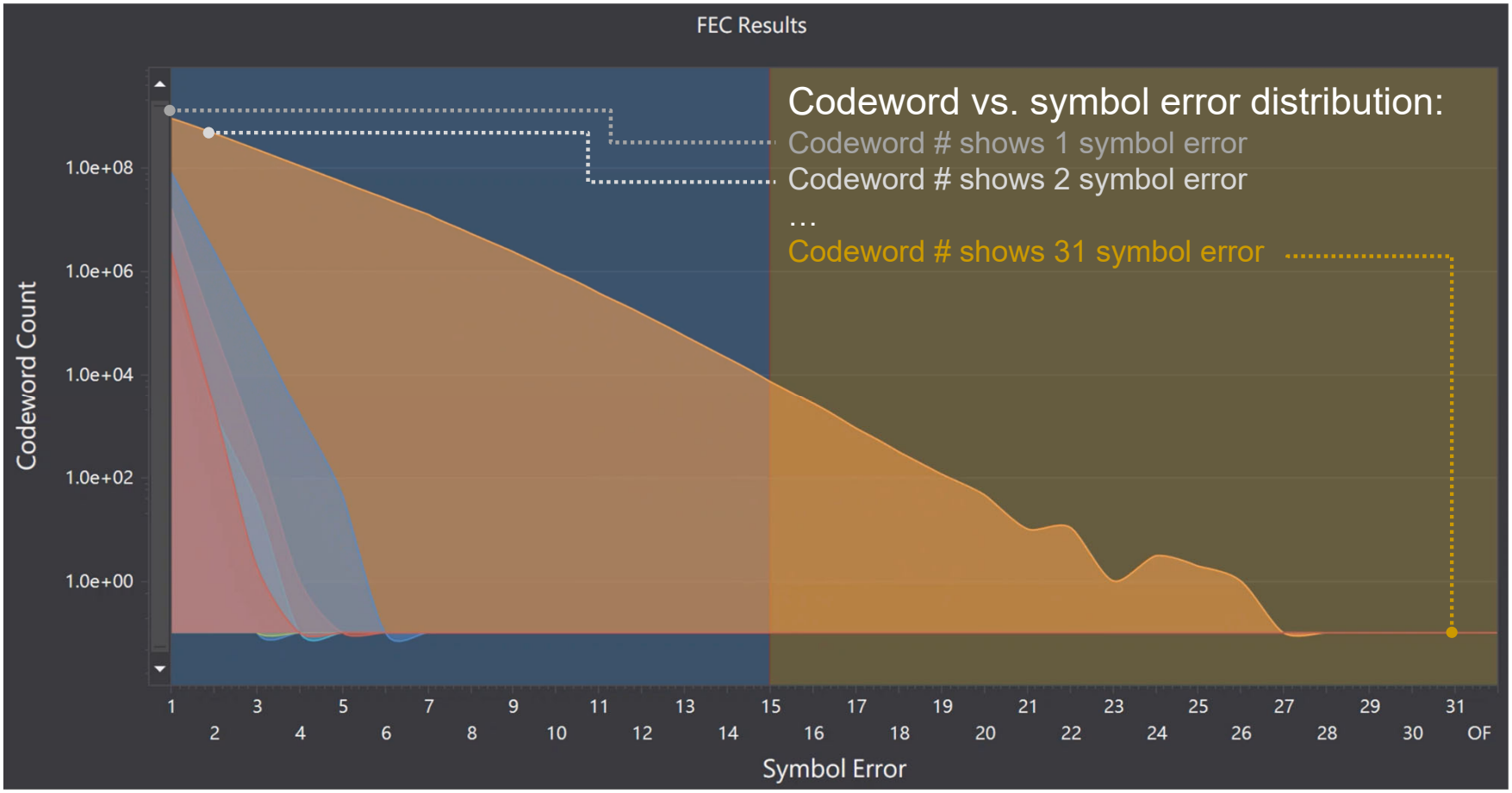
Longer Burst Errors



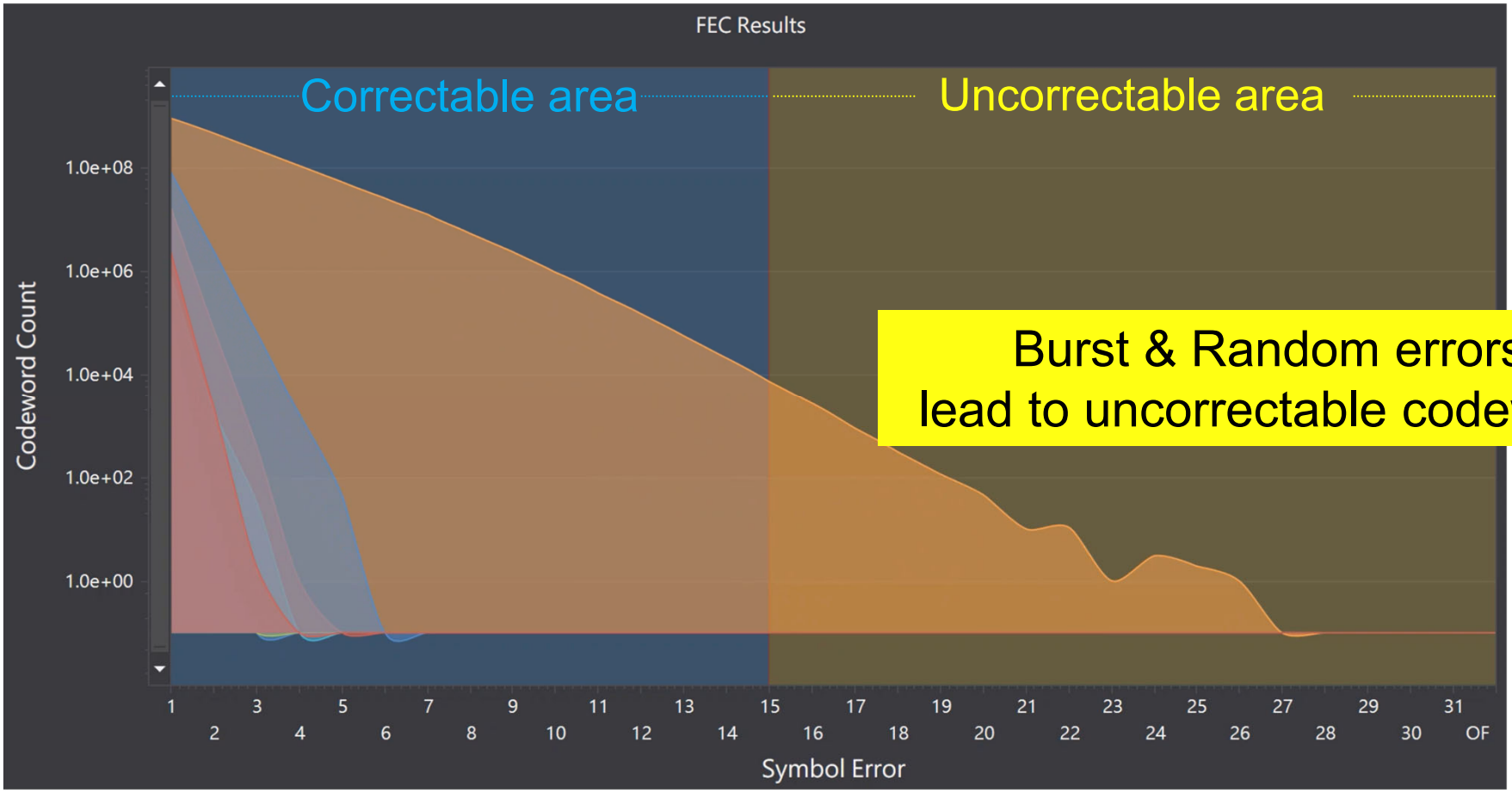
151 bits burst errors in symbols



Symbol error distribution on BA-4000

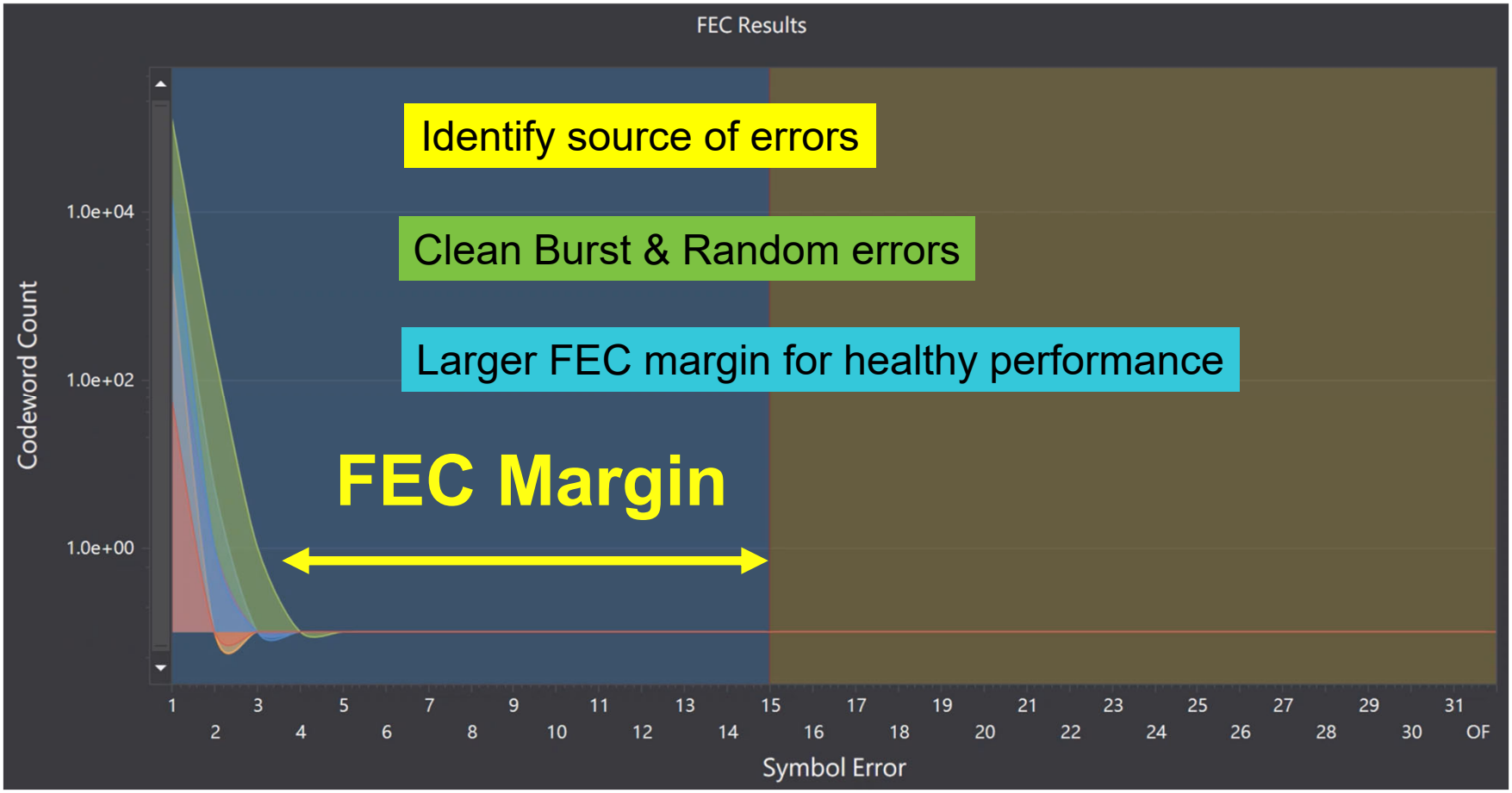


Symbol error distribution on BA-4000



Burst & Random errors
lead to uncorrectable codeword

Symbol error distribution on BA-4000



FEC margin

Key Performance Indicator of 400G and 800G devices


FEC margin testing is critical to fully qualify 400G transceivers on production line.
It improves the compatibility issue between TxRx & switch system.
Tier-1 transceiver vendor

BA-4000
for advanced FEC

BA-4000 provides complete FEC analysis

FEC

FEC Simulator

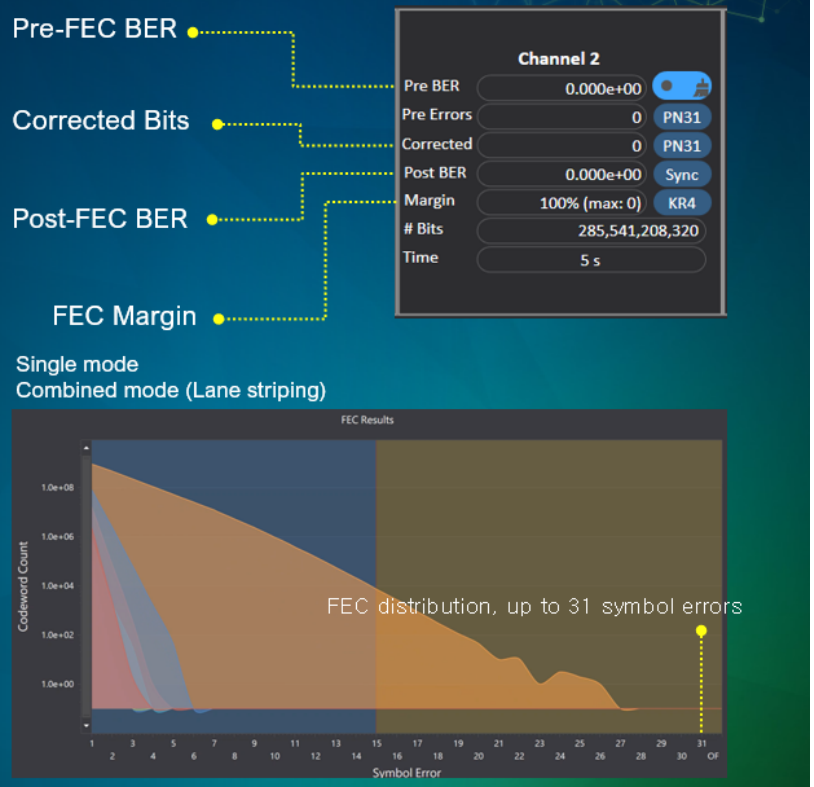
FGC

FEC Generator & Checker

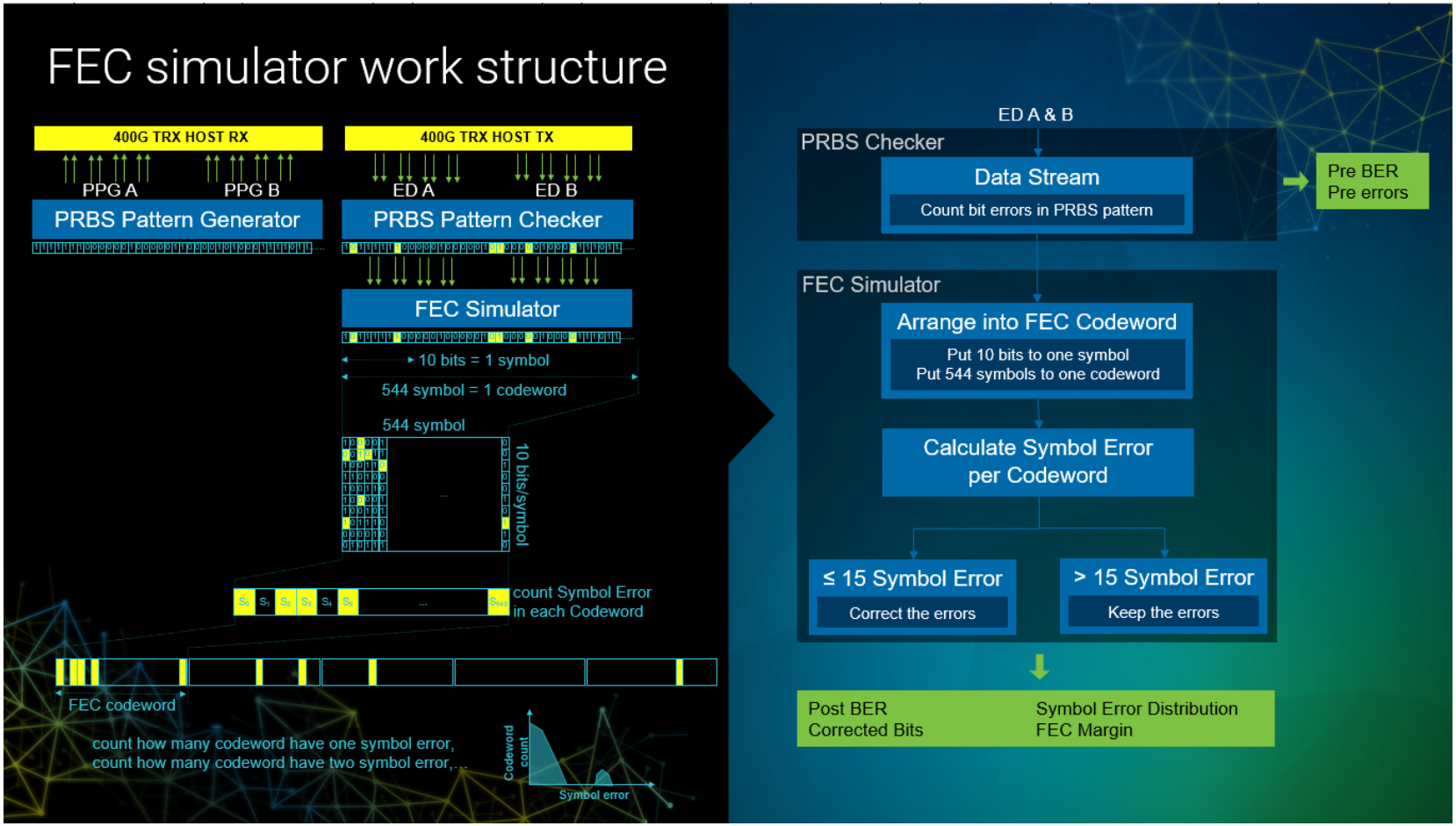
FEC Simulator *FEC4/FEC8 option

- Analyze FEC behavior with only PRBS pattern
  Support 25.78125~28.9GBd PAM4/NRZ;
  51.5625~57.8GBd PAM4/NRZ *FGC4/FGC8 option
- Support combined/single mode, same as real switch strip data to each lane
- Support several RS-FEC protocols:
  KP4/KR4/Low latency

BA-4000 GUI in FEC mode



FEC simulator work structure



FEC Generator & Checker
*FGC4/FGC8 option

- Support **RS-FEC Scrambled Idle pattern**
- Support standardized data rate:

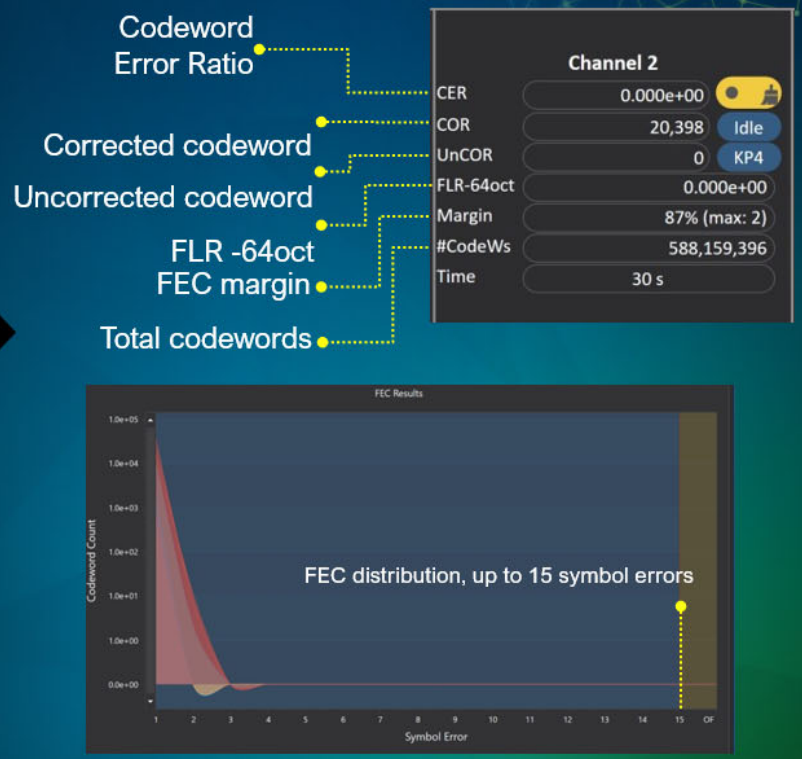
  25.78125GBd NRZ, 26.5625GBd PAM4,

  53.125GBd PAM4
- Analyze product from system overview:

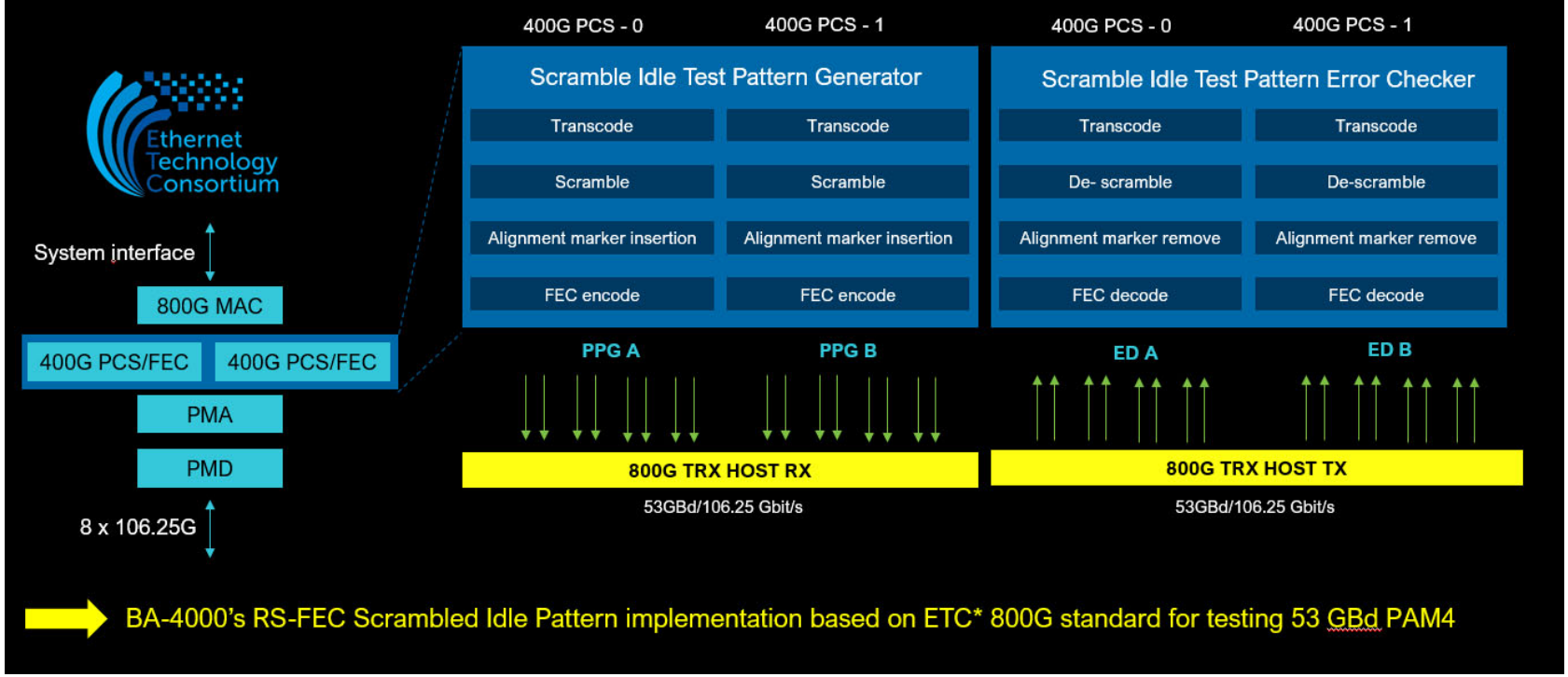
  CER (Codeword Error Ratio), **FEC margin**,

  FLR (64-octet frames with minimum interpacket gap)

BA-4000 GUI in FGC mode

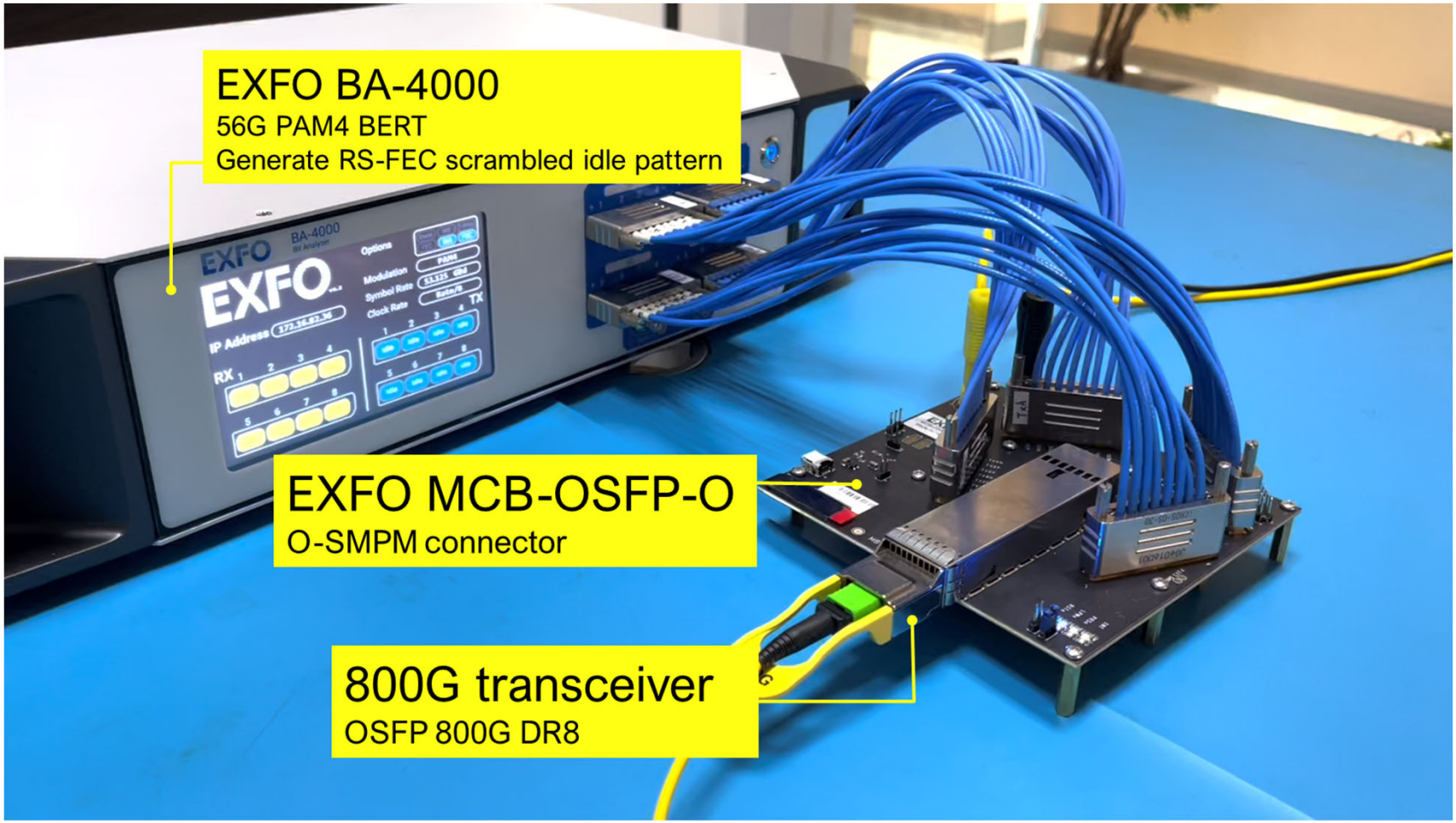


FGC work structure (Scramble Idle Pattern)



BA-4000's RS-FEC Scrambled Idle Pattern implementation based on ETC* 800G standard for testing 53 GBd PAM4

BA-4000: 800G FGC setup



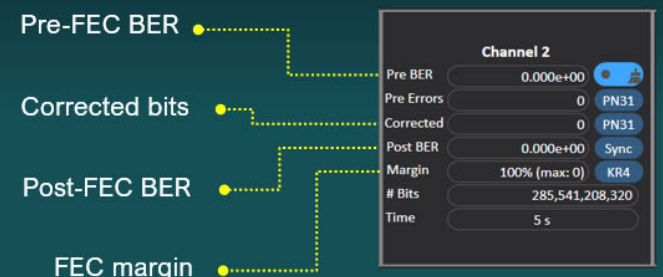
BA-4000: 800G FGC User Interface

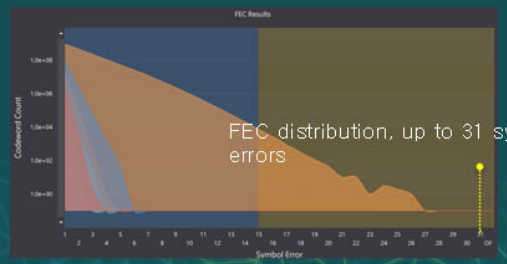
FEC analysis in BA-4000

Analysis tools

FEC Simulator
FEC4/FEC8 option

Pre-FEC BER
Corrected bits
Post-FEC BER
FEC margin

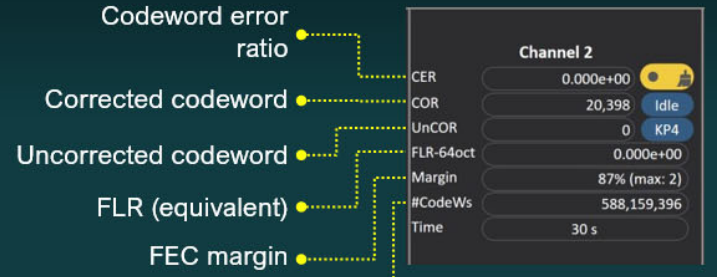


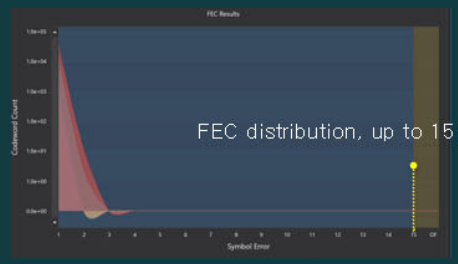


NEW

FEC Generator & Checker
FGC4/FGC8 option

Codeword error ratio
Corrected codeword
Uncorrected codeword
FLR (equivalent)
FEC margin
Total codewords



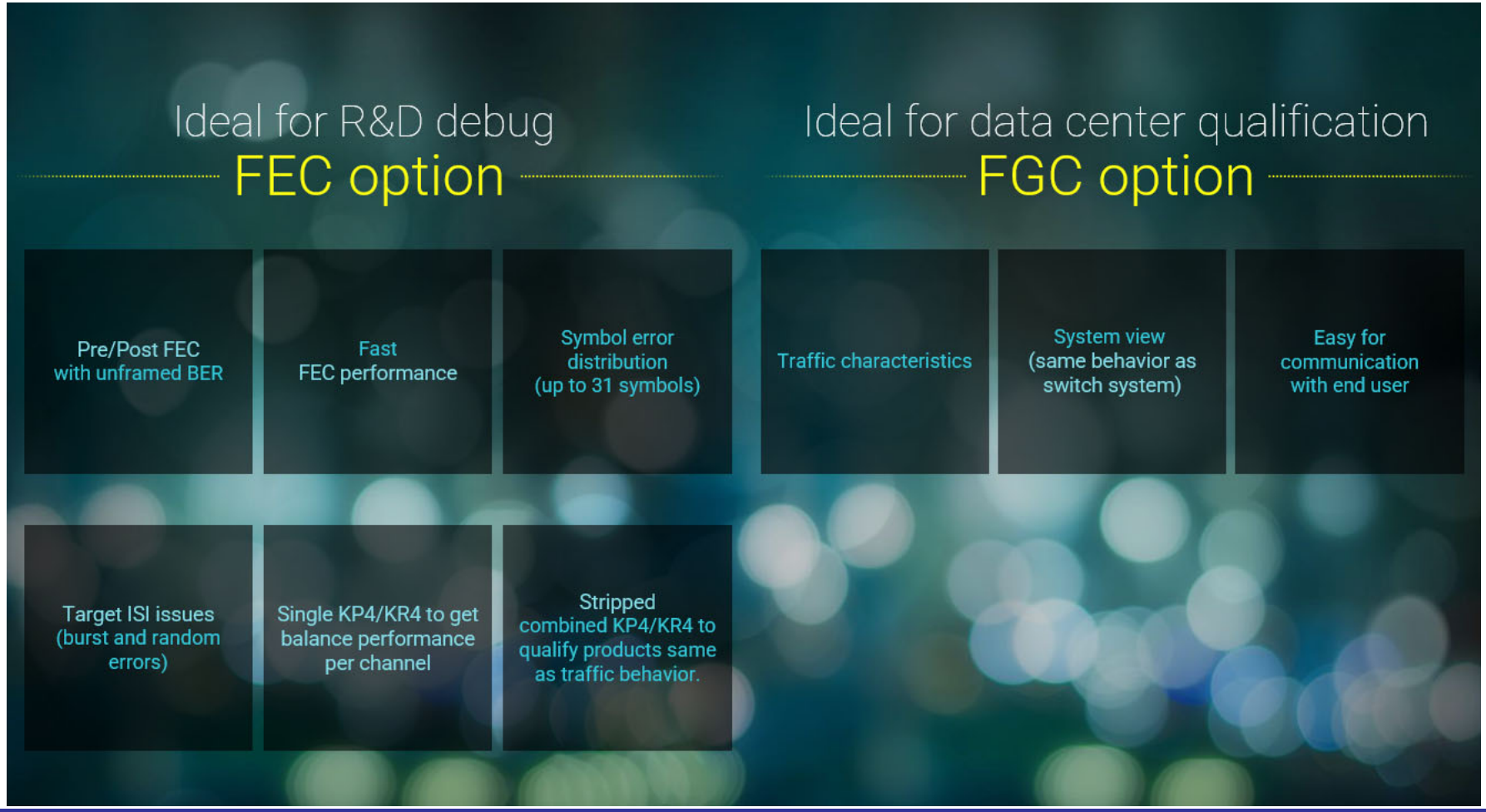


Summary: BA-4000 for advanced FEC

	FEC Simulator FEC4/FEC8 option	NEW FEC Generator & Checker FGC4/FGC8 option
Pattern (Generation & Analysis)	PRBS Pattern	RS-FEC Scrambled Idle Patten (KP4, KR4)
Method of FEC Analysis	Using Layer 1 PRBS Pattern Analysis of Post FEC BER with Bit's approach	Using Layer 1 PCS Scramble Idle with RS-FEC coding Analysis of Codeword Error with Codeword's approach
Data Rate	25.78125~28.9GBd PAM4/NRZ 51.5625~57.8GBd PAM4/NRZ (with FGC option)	25.78125GBd NRZ, 26.5625GBd PAM4, 53.125 PAM4
FEC Type	RS-FEC KP4, KR4, Low Latency	RS-FEC KP4, KR4

Use Cases

Use Cases


Ideal for R&D debug
FEC option
Pre/Post FEC with unframed BER
Fast FEC performance
Symbol error distribution (up to 31 symbols)
Target ISI issues (burst and random errors)
Single KP4/KR4 to get balance performance per channel
Stripped combined KP4/KR4 to qualify products same as traffic behavior.
Ideal for data center qualification
FGC option
Traffic characteristics
System view (same behavior as switch system)
Easy for communication with end user

Key takeaways

- **PRBS testing is a good start**
- **FEC in physical layer**
  Easy to find Burst/Random errors
- **800G FEC metrics**
  Pre/Post FEC, FEC margin, CER, FLR
- **FEC Simulator**
  Analysis of bit behavior per lane
- **FEC Generator & Checker**
  Analysis of system and provides traffic characteristics

Stay tuned!


1
AI/ML driving bandwidth demand
• New 200G/lane transceivers (800G DR4/FR4/LR4, 1.6T DR8)
2
DCI connectivity
• 400G-ZR, 800G-ZR...1.6T-ZR
What's Next?
4
Low Power/Low Latency
• Low power, low latency transceivers (LPO and LRO)
3
Disaggregated Optical Networks
• IPoDWDM leveraging coherent transceivers

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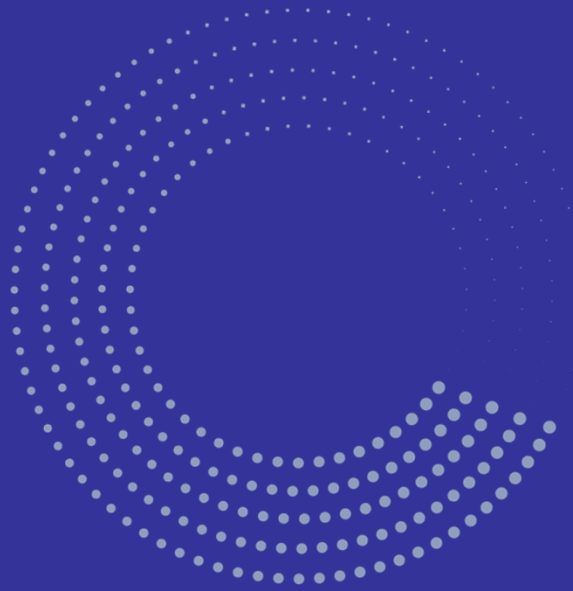
Questions?



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